

Solid State TECHNOLOGY

Insights for Electronics Manufacturing

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BETTER TECHNOLOGY STRONGER TOGETHER

JCET Completes Acquisition of STATS ChipPAC to Ascend to a Leading OSAT Player Globally

China's leading semiconductor packaging and testing company, Jiangsu Changjiang Electronics Technology (JCET, SHE: 600584), successfully completed the acquisition on Aug 5 2015 of STATS ChipPAC, a leading provider of advanced semiconductor packaging and test services headquartered in Singapore. This USD 780 mn transaction was originally announced on Dec 30 2014, and was conducted through JCET-SC (Singapore) Pte. Ltd., a subsidiary of JCET.

This acquisition will escalate the combined entities to one of the world's top outsourced semiconductor assembly and test (OSAT) players. As a combined group of companies, JCET and STATS ChipPAC offer a broader technology portfolio with significant manufacturing scale in key semiconductor geographies. The acquisition will also improve the competitiveness of the Chinese semiconductor packaging and test industry with a strong intellectual property (IP) and innovation portfolio built around advanced technologies acquired by JCET.

"The completion of our acquisition of STATS ChipPAC is an important step for us, and it presents an exciting win-win opportunity for both companies, supporting our long-term success," said Xinchao Wang, Chairman of JCET. "Post acquisition, the combined entities will provide one of the most extensive product/service portfolios to a highly diversified customer base with wide geographical coverage. Our leadership position in advanced packaging technologies will be further strengthened through the acquisition. JCET and STATS ChipPAC are working together to deliver the substantial revenue and cost synergies for our investors."

For more information, visit www.cj-elec.com or www.statschippac.com.





The MAPPER FLX-1200 litho tool in the Leti cleanroom interfaced with a SCREEN DUO track.

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New ways are needed to feed data back and forth between designers, chip fabs, and Out-Sourced Assembly and Test (OSAT) companies.

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Time is a critical element in all phases of semiconductor manufacturing.

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editorial

IoT Surveys Indicate Optimism, Confusion

Solid State Technology recently conducted a survey of our readers on how the Internet of Things (IoT) is driving the demand for semiconductor technology. A total of 303 people responded to the survey. A majority of the respondents were in management roles.

Survey questions focused on their expectations for growth in the Internet of Things (IoT), drivers, potential roadblocks, opportunities and impact on semiconductor technology, including manufacturing and packaging.

"A majority of the respondents said the existing supply chain and industry infrastructure was not equipped to handle the needs of the IoT."

There is little agreement on how strongly the IoT device market will grow. About a quarter of the respondents said, by 2020, 30-50 billion devices would be connected to internet with unique urls. Almost as many were much more optimistic, saying more than 90 billion.

A sizable majority of the respondents (59.41%) believe new companies will emerge to benefit from the growth in IoT. Existing companies will also benefit, with MEMS companies benefitting the most.

A majority of the respondents said the existing supply chain and industry infrastructure was not equipped to handle the needs of the IoT or said they weren't sure. Similarly, most said new manufacturing equipment and new materials will be needed for IoT device manufacturing.

My take on this is that while the market potential for companies involved in IoT devices is large, there is little agreement on exactly how large it might become.

I believe it's also likely that new companies will emerge focused specifically on manufacturing IoT devices. Existing companies across the supply chain will also benefit.

Clearly, IoT devices will create new challenges, especially in the area of packaging. Form-factor, security and reliability are the most important characteristics of IoT devices.

Another recently completed survey on the IoT by McKinsey & Company and the Global Semiconductor Alliance (GSA) revealed some ambiguity about whether the IoT would be the top growth driver for the semiconductor industry or just one of several important forces.

The survey of executives from GSA member companies showed that they had mixed opinions about the IoT's potential, with 48 percent stating that it would be one of the top three growth drivers for the semiconductor industry and 17 percent ranking it first. ♦

—Pete Singer, Editor-in-Chief

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TECHNOLOGY®**

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Web Exclusives

What chipmakers will need to address growing complexity, cost of IC design and yield ramps

As these early days of the Internet of Things show the network's promise and reveal technological challenges that could threaten its ability to meet user expectations in the years ahead, technology providers will be charged with supplying the solutions that will meet those challenges.

<http://bit.ly/1E3NlmR>

Process Watch: The most expensive defect – Part 2

The December 2014 edition of Process Watch suggested that the most expensive defect is the one that goes undetected until the end of line. Indeed, undetected excursions typically result in the scrap of millions of dollars per year of defective semiconductor chips. But many electronics suppliers and OEMs would argue that the consequences of field failures (reliability defects) are much worse than those of non-functioning devices detected at electrical test (killer defects).

<http://bit.ly/1lsQWGN>

Tackling advanced litho challenges on the path to node 5

If you attended just about any mask making conference in the last five to seven years, you would have heard the lament about exploding data volumes and their impact on mask writing time and, by extension, mask costs. The industry is still concerned with data volumes, whether 193nm immersion or EUVL.

<http://bit.ly/1FW02u4>

Move over, 16nm – here comes 10nm chips

Those 16-nanometer chips with FinFETs? Yesterday's news. Taiwan Semiconductor Manufacturing wants you to know that they're ready, willing, and able to help you design chips with 10-nanometer features.

<http://bit.ly/1FF31Z0>



Apple Watch and ASE start new era in SiP

Back in April, the Apple Watch appeared in Chipworks' labs, and of course, they pulled it apart to see its contents.

<http://bit.ly/1WCRpAs>

Insights from the Leading Edge: News from Toshiba, UMC, and Nvidia

In his 250th blog post, Phil Garrou reports on Toshiba extending TSV Memory stacking to NAND, UMC entering HVM on SI interposers for AMD FIJI, and Nvidia's Pascal coming in 2016.

<http://bit.ly/1J2iELI>

Cross-point ReRAM Integration Claimed by Intel/Micron

The Intel/Micron joint-venture now claims to have successfully integrated a Resistive-RAM (ReRAM) made with an unannounced material in a cross-point architecture, switching using an undisclosed mechanism.

<http://bit.ly/1MVhWCR>

SEMICON West: The road forward is 3DIC

SEMICON West 2015 had a strong and rich undercurrent – the roadmap forward is most certainly 3DIC. Yes, the industry can and we will keep pushing dimensions down, but for most designs the path forward would be "More than Moore." As GlobalFoundries' CEO Jha recently voiced: It's clear that More-than-Moore is now mainstream rather than niche.

<http://bit.ly/1KLYPLn>

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- SM8 Bioinspired Metal Nanoparticles—Synthesis, Properties and Application
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news

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USA – FSUSS MicroTec announced new competence-center for nano-imprint in North America.

USA – Qualcomm completed its \$2.4B acquisition of **CSR**.

EUROPE – imec announced plans to extend its GaN-on-Si R&D program, and is now offering joint research on GaN-on-Si 200mm epitaxy and enhancement mode device technology.

ASIA – MagnaChip will host its first Foundry Technology Symposium in Shanghai, China.

USA – Microchip Technology completed its acquisition of **Micrel**.

ASIA – Toshiba launched 16MP CMOS image sensors targeting smartphones and tablets.

EUROPE – CEA-Leti and EV Group launched a new program in nano-imprint lithography called INSPIRE.

ASIA – STATS ChipPAC announced the promotion and appointment of Dr. Han Byung Joon as Co-President and CEO for the company.

USA – Applied Materials unveiled the Applied Olympia ALD system.

EUROPE – CEA-Leti reported FinFET feasibility and circuit design with its CoolCube technology.

USA – Intel announced it will invest \$5 million in its engineering partnership with **Georgia Tech** over the next five years.

Chinese chipmaker Tsinghua prepares \$23B bid for Micron Technology

By Shannon Davis, Web Editor

China's state-owned Tsinghua Unigroup Ltd. is preparing a \$23 billion bid for chipmaker Micron Technology, in what analysts say would be the biggest Chinese takeover of a U.S. company.

Tsinghua, China's largest state-owned chip design company, is prepared to bid \$21 per share for Micron, according to Dow Jones.

As of Tuesday, a Micron spokesman told Reuters that the company had not yet received an offer, while Tsinghua chairman Zhao Weiguo told Bloomberg that the Chinese company was "very interested in cooperation" with Micron.

Tsinghua's potential purchase of Micron is regarded as a strategic move to help the advancement of China's own chip sector. The country currently has no major home-grown memory makers, according to Reuters.

Micron is the last remaining U.S. producer of DRAM memory chips, and any foreign

takeover would still have to pass a review by the Committee on Foreign Investment in the United States, to examine the national security implications of the deal. The deal would also need to be examined by the Chinese National Development and Reform Commission.

This would not be the first significant consolidation in the memory sector this year. In May, Hewlett-Packard sold a 51 percent stake in its data-networking business to Tsinghua for approximately \$2.3 billion.

"Valuation appears low as a potential \$21 a share bid is 8.3 times fiscal year PE or low end of the historic range of 7 to 15 whereas Micron was at \$32 just 5 months ago," UBS analyst Stephen Chin told MarketWatch.

MarketWatch speculated that a cheap valuation could encourage other companies to launch their own bids. ◀

Intel and Micron produce breakthrough memory technology

Intel Corporation and Micron Technology, Inc. unveiled 3D XPoint technology, a non-volatile memory that has the potential to revolutionize any device, application or service that benefits from fast access to large sets of data. Now in production, 3D XPoint technology is a major breakthrough in memory process technology and the first new memory category since the introduction of NAND flash in 1989.

The explosion of connected devices and digital services is generating massive amounts of new data. To make this data useful, it must be stored and analyzed very quickly, creating challenges for service providers and system builders who must balance cost, power and performance trade-offs when they design memory and storage solutions. 3D XPoint technology combines the performance, density, power, non-volatility and cost advantages of all available memory technologies on the market today. The technology is up to 1,000 times faster and has up to 1,000 times greater endurance than NAND, and is 10 times denser than conventional memory.

"For decades, the industry has searched for ways to reduce the lag time between the

Continued on page 8

GLOBALFOUNDRIES completes acquisition of IBM Microelectronics business

GLOBALFOUNDRIES announced that it has completed its acquisition of IBM's Microelectronics business.

With the acquisition, GLOBALFOUNDRIES gains differentiated technologies to enhance its product offerings in key growth markets, from mobility and Internet of Things (IoT) to Big Data and high-performance computing. The deal strengthens the company's workforce, adding decades of experience and expertise in semiconductor development, device expertise, design, and manufacturing. And the addition of more than 16,000 patents and applications makes GLOBALFOUNDRIES the holder of one of the largest semiconductor patent portfolios in the world.

"Today we have significantly enhanced our technology development capabilities and reinforce our long-term commitment to investing in R&D for technology leadership," said Sanjay Jha, chief executive officer of GLOBALFOUNDRIES. "We have added world-class technologists and differentiated technologies, such as RF and ASIC, to meet our customers' needs and accelerate our progress toward becoming a foundry powerhouse."

Through the addition of some of the brightest and most innovative scientists and engineers in the semiconductor industry, GLOBALFOUNDRIES solidifies its path to advanced process technologies at 10nm, 7nm, and beyond.

In RF, GLOBALFOUNDRIES now has technology leadership in wireless front-end module solutions. IBM has developed world-class capabilities in both RF silicon-on-insulator (RFSOI) and high-performance silicon-germanium (SiGe) technologies, which are highly complementary to GLOBALFOUNDRIES' existing mainstream technology offerings. The company will continue to invest to deliver the next generation of its RFSOI roadmap and looks to capture opportunities in the automotive and home markets.

In ASICs, GLOBALFOUNDRIES now has technology leadership in wired communications. This enables the company to provide the design capabilities and IP necessary to develop these high-performance customized products and solutions. With increased investments, the company plans to develop additional ASIC solutions in areas of storage, printers and networking. The most recent ASIC family, announced in January and built on GLOBALFOUNDRIES' 14nm-LPP technology, has been well accepted in the marketplace with several design wins.

GLOBALFOUNDRIES increases its manufacturing scale with fabs in East Fishkill, NY and Essex Junction, VT. These facilities will operate as part of the company's growing global operations, adding capacity and top-notch engineers to better meet the needs of its existing and new customers.

Moreover, the transaction builds on significant investments in the burgeoning Northeast Technology Corridor, which includes GLOBALFOUNDRIES' leading-edge Fab 8 facility in Saratoga County, NY and joint R&D activities at SUNY Polytechnic Institute's College of Nanoscale Science and Engineering in Albany, NY. The company's presence in the northeast now exceeds 8,000 direct employees.

The acquisition includes an exclusive commitment to supply IBM with advanced semiconductor processor solutions for the next 10 years. GLOBALFOUNDRIES also gets direct access to IBM's continued investment in semiconductor research, solidifying its path to advanced process geometries at 10nm and beyond. ◀

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IBM Research alliance produces industry's first 7nm node test chips

IBM Research announced that working with alliance partners at SUNY Polytechnic Institute's Colleges of Nanoscale Science and Engineering (SUNY Poly CNSE) it has produced the semiconductor industry's first 7nm (nanometer) node test chips with functional transistors. The breakthrough underscores IBM's continued leadership and long-term commitment to semiconductor technology research.

The accomplishment, made possible through IBM's unique public-private partnership with New York State and joint development alliance with GLOBALFOUNDRIES, Samsung and equipment suppliers, is driven by the company's \$3 billion, five-year investment in chip R&D announced in 2014. Under that program, IBM researchers based at SUNY Poly's NanoTech Complex in Albany are pushing the limits of chip technology to 7nm node and beyond to meet the demands of cloud computing and Big Data systems, cognitive computing and mobile products.

Developing a viable 7nm node technology has been one of the grand challenges of the semiconductor industry. Pursuing such small dimensions through conventional processes has degraded chip performance and negated the expected benefits of scaling — higher performance, less cost and lower power requirements. Microprocessors utilizing 22nm and 14nm technology power today's servers, cloud data centers and mobile devices, and 10nm technology is well on the way to becoming a mature technology, but 7nm node has remained out of reach due to a number of fundamental technology barriers. In fact, many have questioned whether the traditional benefits of such small chip dimensions could ever be achieved.

The IBM 7nm node test chip with functioning transistors was achieved using new semiconductor processes and techniques

pioneered by IBM Research. Developing it required a number of first-in-the-industry innovations, most notably silicon germanium (SiGe) channel transistors and extreme ultraviolet (EUV) lithography integration at multiple levels.

By introducing SiGe channel material for transistor performance enhancement at 7nm node geometries, process innovations to stack them below 30nm pitch and full integration of EUV lithography at multiple levels, IBM was able to achieve close to 50 percent area scaling improvements over today's most advanced 10nm technology. These efforts could result in at least a 50 percent power/performance improvement for the next generation of systems that will power the Big Data, cloud and mobile era.

The 7nm node milestone continues IBM's legacy of historic contributions to silicon and semiconductor innovation. They include the invention or first implementation of the single cell DRAM, the Dennard Scaling Laws, chemically amplified photoresists, copper interconnect wiring, Silicon on Insulator, strained engineering, multi core microprocessors, immersion lithography, high speed SiGe, High-k gate dielectrics, embedded DRAM, 3D chip stacking and Air gap insulators.

IBM and SUNY Poly have built a highly successful, globally recognized partnership at the multi-billion dollar Albany NanoTech Complex, highlighted by the institution's Center for Semiconductor Research (CSR), a \$500 million program that also includes the world's leading nanoelectronics companies. The CSR is a long-term, multi-phase, joint R&D cooperative program on future computer chip technology. It continues to provide student scholarships and fellowships at the university to help prepare the next generation of nanotechnology scientists, researchers and engineers. ◀

Intel and Micron, Continued from page 6

processor and data to allow much faster analysis," said Rob Crooke, senior vice president and general manager of Intel's Non-Volatile Memory Solutions Group. "This new class of non-volatile memory achieves this goal and brings game-changing performance to memory and storage solutions."

"One of the most significant hurdles in modern computing is the time it takes the processor to reach data on long-term storage," said Mark Adams, president of Micron. "This new class of non-volatile memory is a revolutionary technology that allows for quick access to enormous data sets and enables entirely new applications."

As the digital world quickly grows—from 4.4 zettabytes of digital data created in 2013 to an expected 44 zettabytes by 20204

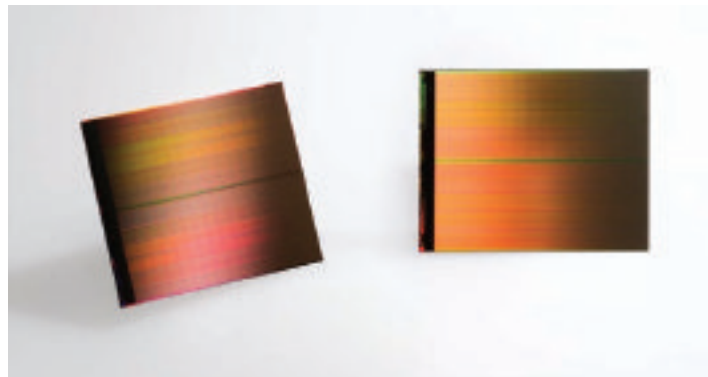
– 3D XPoint technology can turn this immense amount of data into valuable information in nanoseconds. For example, retailers may use 3D XPoint technology to more quickly identify fraud detection patterns in financial transactions; healthcare researchers could process and analyze larger data sets in real time, accelerating complex tasks such as genetic analysis and disease tracking.

The performance benefits of 3D XPoint technology could also enhance the PC experience, allowing consumers to enjoy faster interactive social media and collaboration as well as more immersive gaming experiences. The non-volatile nature of the technology also makes it a great choice for a variety of low-latency storage applications since data is not erased when the device is powered off.

New recipe, architecture for breakthrough memory technology

Following more than a decade of research and development, 3D XPoint technology was built from the ground up to address the need for non-volatile, high-performance, high-endurance and high-capacity storage and memory at an affordable cost. It ushers in a new class of non-volatile memory that significantly reduces latencies, allowing much more data to be stored close to the processor and accessed at speeds previously impossible for non-volatile storage.

The innovative, transistor-less cross point architecture creates a three-dimensional checkerboard where memory cells sit at the intersection of word lines and bit lines, allowing the cells to be addressed individually. As a result, data can be written and read in small sizes, leading to faster and more efficient read/write processes.



3D XPoint technology will sample later this year with select customers, and Intel and Micron are developing individual products based on the technology. ◀▶

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New AMS Fab Going to Marcy NY

Austria-based ams AG, formerly known as Austriamicrosystem, announced plans to locate a new 360,000 ft² fab in upstate New York at the Nano Utica site in Marcy, NY. The fab will be used to manufacture analog devices on 200/300mm wafers. Total build-out at the site, including support buildings and office space, will be close to 600,000ft².

This will be the first fab going into the 428 acre Marcy site, which is large enough to accommodate three fabs and an R&D or packaging facility.

Construction of the ams fab is scheduled to begin in spring 2016, with first wafer ramp in the last quarter of 2017.

In what might become the new business model for fabs, the building itself will be publicly owned and leased to ams, which will assume operating costs and most of the costs of the capital equipment. Capital purchases, operating expenses and other investments in the facility over the first 20 years are estimated at more than \$2 billion. ams will create and retain more than 700 full time jobs and anticipates the creation of at least 500 additional support jobs from contractors, subcontractors, suppliers, and partners necessary to establish the full ecosystem necessary to enable advanced manufacturing operations.

Fort Schuyler Management (FSMC) will handle the construction, with the goal of turning the fab over to ams in Q2 2017. A key part of N.Y. Governor Cuomo's START-UP NY initiative, FSMC is a State University of New York (SUNY Polytechnic Institute) affiliated, private, not-for-profit, 501c(3) corporation that facilitates research and economic development opportunities in support of New York's emerging nanotechnology and semiconductor clusters.

"If jobs are being created, everything else will take care of itself," Cuomo said.

Mohawk Valley EDGE President Steve DiMeo said site work has already started. "We're putting roads in, storm drainage, utilities and we just approved the change order for clearing the land where ams will be located. We'll be doing some additional site development this fall, and work closely with Fort Schuyler so that they will be in a position to begin construction the early part of next year."

In a related announcement, GE Global Research said it will expand its New York global operations to the Mohawk Valley, serving as the anchor tenant of the Computer Chip Commercialization Center (QUAD C) on the campus of SUNY Polytechnic Institute's Colleges of Nanoscale Science and Engineering in Utica. Nearly 500 jobs are expected to be created in the Mohawk Valley in the next five years from SUNY Poly, GE and affiliated corporations and another 350 in the subsequent five years.

These public-private partnerships represent the launch of the next phase of the Governor's Nano Utica initiative, which now exceeds more than 4,000 projected jobs over the next ten years. Designed to replicate the dramatic success of SUNY Poly's Nanotech Megaplex



An artist's rendering of what a fab would look like at the Marcy site.

in Albany, NANO Utica further cements New York's international recognition as the preeminent hub for 21st century nanotechnology innovation, education, and economic development.

"This is a transformative moment that will make a difference in peoples' lives in the Mohawk Valley for generations to come," said Governor Cuomo. "Over the past few years, we have worked to reverse the negative and invest in Upstate NY – and today we're taking another huge step forward. With GE and ams joining the Nano Utica initiative, we're seeing the region's economy gathering momentum unlike ever before. The Mohawk Valley is beginning an economic revolution around nanotechnology, and I am excited to see the region take off and thrive, both today and in the years ahead."

Dr. Alain Kaloyeros, President and Chief Executive Officer of SUNY Polytechnic Institute, said, "Today's announcement by Governor Andrew Cuomo represents a major expansion for Quad-C and the Nano Utica initiative and is a tremendous victory for the Mohawk Valley and the entire State of New York. World renowned partners such as GE Global Research and AMS raise the level of prestige for the entire region and accelerate the development of this international hub for technology and innovation. Governor Cuomo's pioneering economic development model, coupled with SUNY Poly CNSE's world class expertise and resources, continues to generate historic investment and job creation throughout the state. We welcome GE and AMS and their leadership teams and look forward to their partnership in the continued growth of Nano Utica."

ams Chief Operating Officer Dr. Thomas Stockmeier said, "Building a new wafer fab will help us achieve our growth plans and meet the increasing demand for our advanced manufacturing nodes. Our decision to locate the facility in New York was motivated by the highly-skilled workforce, the proximity to esteemed education and research institutions, and the favorable business environment provided by Governor Cuomo and all the public and private partners we are working with on this important project."

Additionally, ams will collaborate with FSMC and SUNY Poly on a joint development program to support complimentary research, commercialization and workforce training opportunities at SUNY Poly facilities throughout New York State. ◀▶

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Advances in thermo-compression bonding

At the 65th IEEE ECTC, several companies presented advances in thermos-compression bonding.



PHIL GARROU,
Contributing Editor

Jie Fu of Qualcomm discussed “Thermal Compression Bonding for Fine Pitch Solder Interconnects.” Mass reflow-based interconnects, using either solder bump or Cu-column on bond on lead are the typical low-cost flip chip assembly approaches used by industry. These interconnects face challenges related to shorting and non-wets at sub 100 μ m pitches. Transitioning below 100 μ m pitch requires a new approach, such as thermos-compression flip chip (TCFC). While TCFC provides higher accuracy bonding and allows for use of smaller solder cap which enables tighter FC pitch, it also presents new challenges. The major challenges for TCFC bonding include lower throughput and control of non-conductive paste (NCP) voids.

Overall, bond head ramp rate, temperature uniformity, peak temperature and dwell time must be fine-tuned in tandem to compensate for manufacturing tolerances and to get the desired end of line solder joint structure. In addition, controlling the temp exposure for the NCP material before NCP cure is critical to enable a robust TCFC solder joint. Too much thermal exposure and the NCP begins to cure prior to solder melting, which can lead to NCP entrapment and unreliable TCFC solder joints. Laminate surface finish is also an important variable.

In a similar study Cho and co-workers at GlobalFoundries presented “Chip Package Interaction Analysis for 20-nm Technology with Thermo-Compression Bonding with Non-Conductive Paste.” Strong market demand for finer pitch interconnects to enable higher I/O counts in a smaller form factor is driving another transition from conventional MR bonding process to thermo-compression bonding using non-conductive paste (TC-NCP). FEA simulation results for TC-NCP vs mass reflow show that TCNCP has significantly reduced thermo-mechanical stress at the ULK level and the bump level.

Horst Clauberg of K&S discussed “High Productivity Thermo-compression Flip Chip Bonding.” There is tremendous effort by IDMs, OSATs, materials suppliers and equipment suppliers to bring thermos-compression bonding to commercial reality. The most significant technical challenges have for the most part

been solved and limited commercial production is taking place. However, relatively low throughput and high equipment cost create adoption resis-

tance, especially in the all-important consumer market.

Thermocompression bonding can be segmented into two different processes. The first process differentiation is whether the underfill is pre-applied before the semiconductor chip is mounted or not. Pre-applied underfill comes either as a film applied to the die or as a paste applied to the substrate. In both cases the underfill must not only create a void-free bond, but also provide flux to remove oxide on the solder caps. The alternative process is thermocompression – capillary underfill (TC-CUF) where the die is underfilled in the same way as standard flip chip, except that the underfill process is much more challenging because of the more narrow bondline of a typical thermocompression bonded device. In TC-CUF, flux can be applied either by dipping the die into flux before bonding, or applying flux to the substrate.

Doug Hiner in a joint presentation between Qualcomm and Amkor presented “Multi-Die Chip on Wafer Thermo-Compression Bonding Using Non-Conductive Film.” Non-conductive films have been in development as a replacement to the liquid preapplied underfill materials used in fine pitch copper pillar assembly.

Several assembly methods are available for chip on wafer assembly including: (1) traditional chip attach with mass reflow (MR) and capillary underfill (CUF), (2) thermo-compression bonding (TCB) of copper pillar interconnects using nonconductive paste (NCP) underfill (TCB+NCP), and thermocompression bonding of copper pillar with non-conductive film (NCF) underfill (TCB+NCF).

The TCB+NCP process carries concerns with the underfill time on stage which prevents the dispensing of the NCP material across the wafer prior to the chip bonding process. This constraint effects process costs significantly. The TCB+NCF process to date have not met the cost/benefit needs of the industry. NCF assembly provides significant improvements in the design rules associated with die to package edge, die to die, and fillet size. The NCF process also resolves the time on stage concerns associated with the NCP process by laminating the NCF material to the bonded die instead of to the interposer or receiving wafer surface. ◀

Packaging



The IoT and the next 50 years of Moore's Law

Fifty years of technological developments following Moore's Law has changed our world in some phenomenal ways, but Intel's Doug Davis believes the time has come to change the way we think about developing new solutions.

At SEMICON West 2015, Intel's Internet of Things Senior Vice President and General Manager challenged attendees to broaden their thinking on the potential of the IoT and examine their own roles in bringing about global change through new, innovative technology.

"The question is not how do we make these devices smart? The question becomes what are the problems that we can work together to solve?" Davis said.

Davis' presentation addressed four complex issues the world is currently facing: an aging population, climate change, the urban boom, and how we feed the planet, offering real IoT solutions that could impact these growing concerns.

IoT and an aging population

Since 1950, the average lifespan has increase by more than 20 years. By the year 2050, more people on the planet will be over the age of 60 than under the age of 14.

"As we're all living healthier, longer lives, we also have to reflect that as a society we're unprepared to provide care for these kinds of numbers," said Davis.

Even if the infrastructure were available, if you talk to seniors, they'd rather live out their lives at home, Davis pointed out. How can the IoT help us with this challenge?

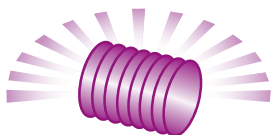
IoT and climate change

No matter where you stand on global warming, there's no arguing that air quality is becoming a serious issue in an increasing number of cities in the world, Davis said.

He challenged his audience to also think about this problem differently, posing the question, "What if we

reduced emissions at every point in the supply chain?"

Semiconductors



SHANNON DAVIS,
Web Editor

Davis cited Intel's own predictive analytics solutions, which have been used in a number of their fabs around the world.

"Engineers at one Intel fab have used this data to reduce maintenance time by 50%, parts replacement by 20%," Davis said. "They were able to reduce non-genuine yield loss by as much as 20%."

With this kind of increase in efficiencies, Davis said Intel believes this also helps to reduce their carbon footprint.

IoT and the urban boom

"We're undergoing the fastest rural to urban migration in human history," Davis explained. "City populations are growing by 65 million people per year – that's seven new Chicagos every year."

And there are a lot of growing concerns that go along with this boom, from traffic problems to pollution. To address these issues, Davis said Intel has pilot programs now in the UK that are beginning to capture data on traffic patterns, air quality, water supply and more, and overlaying that data with public service agencies, which would allow these agencies and eventually citizens to make real-time decisions and changes.

IoT and how we feed the planet

Davis argued that the real problem the world is facing isn't how to feed the planet, but the amount of food wasted while so many people go hungry.

"The World Bank says that we're currently wasting 1/4 to 1/3 of the food that's being produced on the planet today," said Davis. "We have to get better at distributing food."

Davis shared one example of improved agricultural performance through IoT solutions installed in rice fields in Malaysia, where farmers used ground water and weather forecasting analytics to monitor and make decisions about crop management. In the end, Davis said, farmers were able to see water savings of up to 10% and rice production increase of 50%.

"The genius of Moore's Law showed us what was possible and set the pace for us," Davis said. "Over the next 50 years, think about what's possible – think beyond just the device and into the end-to-end solutions we can create, and we can tackle these huge challenges worldwide." ◀

Lithography alternatives: Why are they essential?

LAURENT PAIN, RALUCA TIRON, LUDOVIC LATTARD, STEFAN LANDIS and CYRILLE LAVIRON,

CEA-Leti, Grenoble, France

The availability of patterning alternatives in the lithography landscape represents a big opportunity to properly address the coming needs generated by the IoT.

The Internet of Things (IoT) is expected to fuel significant growth opportunities for the semiconductor industry, as demand increases for wireless components and more and more embedded functionalities such as memory and sensors. This growth will affect almost all integrated circuit (IC) sectors (**FIGURE 1**). The chip industry will continue to need advanced technologies to provide the most powerful functionalized ICs with lower power consumption for the IoT, but manufacturing costs remain a key challenge. Lithography and related patterning technologies can represent up to 50 percent of total IC production costs, and significant efforts have to be made in the coming years to slow and even reverse this trend.

In the lithography landscape for the development of advanced technology nodes, extreme-UV (EUV) lithography technology recovered some credibility

at the beginning of 2015 with the release and installation of the first 80W power sources[1]. However, its adoption by the industry remains uncertain, because its infrastructure still requires significant development. Also, the recurrent questions about the real cost of ownership associated with the ability of the 0.33NA platform to address sub-7nm technology nodes continue to dominate the debate in the semiconductor community, especially since 3D-stacking strategies are being seriously investigated. This potentially could slow demand for high-resolution and therefore delay the new advanced lithography solutions.

Meanwhile, 193nm immersion lithography, with double- or quadruple-patterning strategies, supports the industry preference for advanced-node developments, despite the tremendous effort required for process controls (alignment, mask manufacturing etc.). In this landscape, lithography alternatives maintain promise for continued R&D because they may present competitive compromises for the industry. Massively parallel electron-beam and nano-imprint lithography techniques remain highly attractive, as they can provide noteworthy cost-of-ownership benefits for IC manufacturers. In addition, directed self-assembly (DSA) lithography with block copolymer shows promising resolution capabilities and appears to be an option to reduce multi-patterning strategies, and therefore the associated mask-set budgets. But what is the current status of these technologies? Are they really able to meet

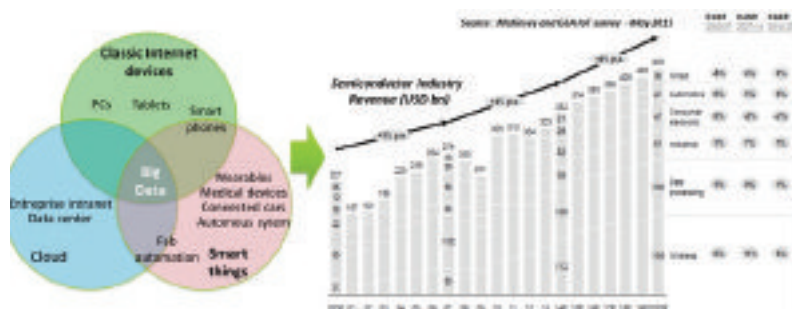


FIGURE 1. Impact of the IoT on semiconductor industry revenue from 2000 to 2020.

LAURENT PAIN is lithography program manager at Leti, **RALUCA TIRON** is head of the IDEAL program, **LUDOVIC LATTARD** is head of the IMAGINE program, **STEFAN LANDIS** is head of the INSPIRE program and **CYRILLE LAVIRON** is lithography laboratory manager at Leti.



FIGURE 2. CEA-Leti schematic on DSA process environment validation

industry expectations for advanced technology nodes? Are they indeed able to reduce manufacturing costs? What are their introduction points into the production environment?

CEA-Leti is working to answer these questions and has initiated collaborative R&D programs to assess and boost the development of these alternative technologies through strategic partnerships. Three programs have been launched with the primary goals of demonstrating that these lithography options can meet industry needs, assessing industrial use of them and proposing to Leti's IDM partners real turn-key integrated process-flow solutions.

- **IMAGINE:** launched in 2009 with MAPPER Lithography, this program is pushing for the insertion of massively parallel direct-write electron-beam technology. Other participants include TSMC, STMicroelectronics, Nissan Chemical, Mentor Graphics, SCREEN, Tokyo Electron and Aselta Nanographics.
- **IDEAL:** DSA lithography represents a promising solution for advanced patterning. Leti has worked with Arkema since 2011 on the qualification and demonstration of materials for insertion into industrial production flow. Other partners include ST, Tokyo Electron, SCREEN, Mentor Graphics and CNRS-LCPO.
- **INSPIRE:** established in 2015 with the EV Group, this program will focus on the assessment of imprint technology on large-scale patterning.

Directed self assembly: the resolution is in polymer matrix

Since 2010, DSA has steadily attracted attention of R&D laboratories and the IDM industry. The natural high-resolution capability of the block copolymer (sub-10nm) may meet the requirements of future technology nodes. Significant work in this area is underway at R&D consortia such as imec, IBM Research in Albany, N.Y., and Leti, as well as directly in the fab[2,3]. For example, Leti and its partners put in place a full infrastructure to qualify the new material developed by the chemical company Arkema (**FIGURE 2**). A full 300mm line is operational at Leti using a Tokyo Electron track and a customized SCREEN DUO track able to handle the latest process possibilities. This type of infrastructure is required to validate in fab-like conditions the new materials (PS-PMMA and high chi platforms) and their associated integration flows. Those operating conditions give industry the capability to quickly evaluate the full process-flow performances with all the required classic statistical data for final validation.



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FIGURE 3. DSA defectivity trend on lamellar. Courtesy T Younkins (Intel) - Private communication.

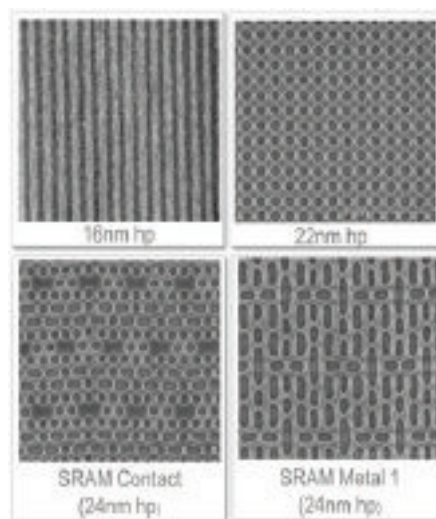


FIGURE 6. Example of MAPPER Lithography patterning capability on the pre-alpha platform[5]

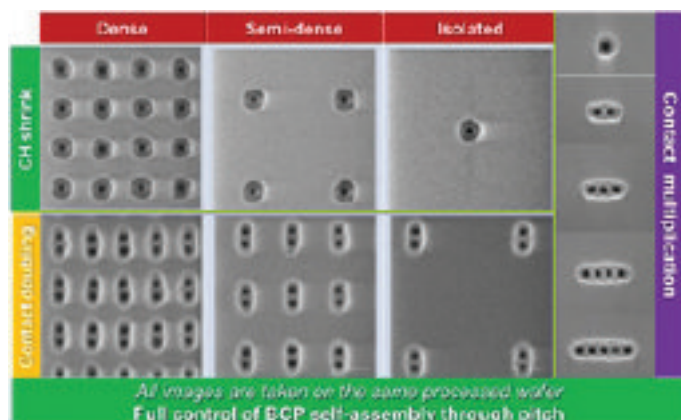


FIGURE 4. Control of iso-dense bias density in Leti DSA

	Not optimized surface affinity control	Optimized surface affinity control
Hole Open Yield	93%	100%
CDU _{DSA} (3σ)	20 %	4.9 %
Placement Error	1.5 nm	0.9 nm
CDU _{DSA} mapping		

FIGURE 5. Influence of surface affinity on key manufacturing-process parameters

Focusing on defectivity Intel showed convincing data at 1def/cm² on line-and-space structures, confirming the potential of DSA to reach the ITRS target and therefore to be used for manufacturing in the near future (**FIGURE 3**). As well, Leti results on grapho-epitaxy process are also very encouraging with zero visual-defect process flow for contact/via application measured with low statistical level[4]. Those results are the first positive key trends in the DSA technology. Evaluating the compatibility of DSA with semiconductor process flows is the next important step. The control of the iso-dense configuration focused

a lot of attention on the grapho-epitaxy process, in which block copolymer film-filling uniformity is affected by the topography effects of the guide patterns. Leti developed and patented a flow allowing a proper control of CD and CDU in all density configurations. (**FIGURE 4**) This solution preserves the interest of DSA as it is integrated in the process flow itself and because it does not imply a need for any additional design-rule restriction[4].

Nevertheless, some hurdles remain to be overcome before its final adoption. The control of the surface affinity is one key aspect. It can greatly affect the final defectivity level and impact the complexity of the integration flow (**FIGURE 5**). Any non-uniform control of the bottom residual polymer thickness in the bottom of the guide cavity may lead to post-etch opening issues and final circuit-yield drop. Moreover, to be fully adopted, DSA technology also must be aligned with the compatible design rule manuals. Insertion in the DRM is essential and it implies adding new specific constraints due to the nature of the block copolymer and to the lithography guide realization. All these R&D efforts must be pushed to value the advantages of DSA technology: the natural high resolution of this solution and its cost effectiveness from reducing multi-exposure strategy. In addition to ensuring DSA's ability to extend 193nm immersion lithography, it also supports the use of the EUV 0.33NA tool for the development of 7nm nodes and below.

Massively parallel electron-beam writing

Despite recurrent delays in new developments, parallel electron-beam lithography remains an attractive alternative option. The massively parallel writing solutions developed by MAPPER Lithography and IMS Nanofabrication for wafer and mask writing, respectively, offer good compromises: a significant alliance of resolution and

advantageous manufacturing costs. But this technology also benefits from additional advantages, such as writing flexibility and a significant throughput improvement due to the parallel exposure concept that can boost the throughput in the future up to 100 wafers per hour in a cluster-tool configuration. First pre-industrial units are today installed in pilot-line environments, foreshadowing their introduction into production lines in coming years.

MAPPER and Leti's collaboration is focused on introducing this technology for direct-write application. This joint program started in 2009 around the MAPPER's pre-alpha tool that validated the key concept of the MAPPER technology in terms of parallel writing and resolution capabilities (**FIGURE 6**). The partnership entered in a new phase in 2014 with the installation of the first FLX-1200 pre-production platform, (**FIGURE 7**), operating 1,300 beam lines for a targeted throughput of 1 wph and then scalable to 10 wph by increasing the beam line count up to 13,000.

This FLX-1200, which is being ramped up now, already has shown imaging performances that match its specifications. Full 300mm wafers can be printed in one hour with 32nm half-pitch resolution (**FIGURE 8**). In the IMAGINE program, Leti and its partners are also working to validate a complete turn-key integrated solution allowing fast and secure wafer processing from design to silicon. Such infrastructure developments around data treatment, materials, process, etch and metrology will be required to speed-up the insertion of the MAPPER technology into future production lines.

Leti and MAPPER will demonstrate the operational



FIGURE 7. MAPPER FLX-1200 in Leti cleanroom interfaced with a SCREEN DUO track. Key figures of the tool: Acceleration voltage 5kV; throughput: 1wph with 1,300 beamlines; resolution/alignment specs: 32nmhp / 10nm 3 σ .

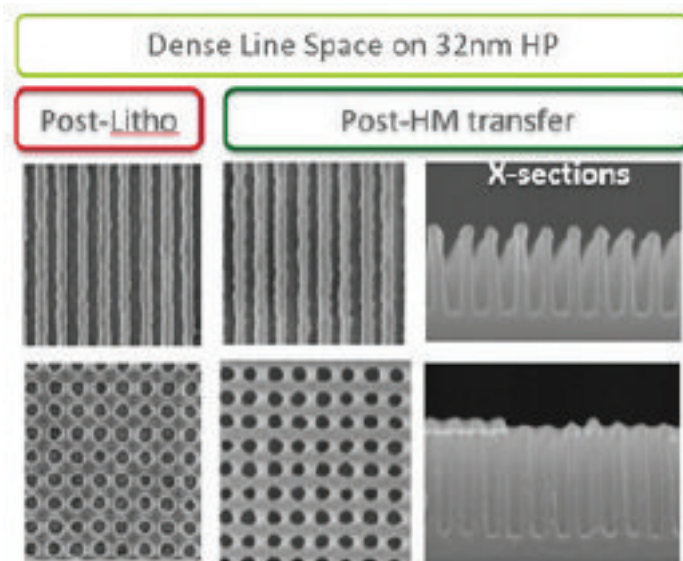


FIGURE 8. First imaging performance of the FLX-1200 on full 300mm wafer

capability of the FLX-1200 in its final configuration, including mix-and-match alignment performances. The achievement of this key demonstration milestone is essential to launching this technology. Then, after final ramp-up, the MAPPER platform is expected to be aligned in terms of specifications with 14nm technology (32nm hp). A wide range of potential applications based on its mask-less concept and throughput potential already have been clearly identified: CMOS prototyping and low-volume production, complementary lithography concept for high-end patterning[6], new industry segments (photonics, low-cost circuit functionalization, large field exposure, etc.).

Nano-imprint lithography

Nano-imprint lithography (NIL) stands out from the other conventional lithography processes (photolithography, electronic lithography, EUV lithography) because of the fundamental mechanism of creating the final structures. In the case of nano-imprint, the flow of the resist directly shapes the pattern through the stamp cavities, eliminating the need for chemical contrast, as is the case for optical lithography resists. In recent decades, significant efforts have been made to extend the distance between the photomask and the resist-coated wafer to reduce defectivity and enhance resolution. Therefore, for many scientists, NIL technology appeared to be a UFO, since the process is based on the intimate contact between the working stamp and the resist to be embossed.

In the past 20 years, significant progress has been made to make the technology more mature and ready for high-volume manufacturing. Among the several existing

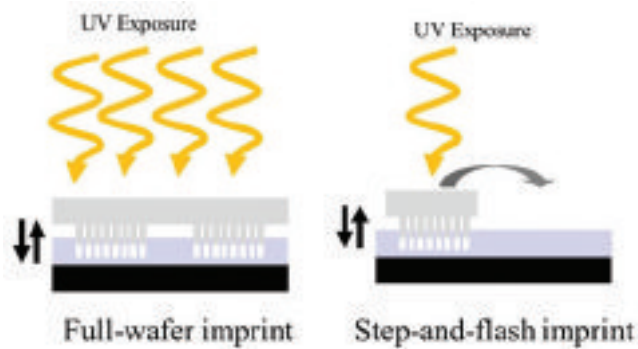


FIGURE 9. Schematic description of the full-wafer and step-and-flash imprint options.

NIL technology alternatives, the UV-based imprint, using transparent stamp, is today the standard one. Two well-established options are now available on the market: the full-wafer imprint (the size of the stamp corresponds to the size of the wafer to be printed) and the step-and-flash imprint in which a small stamp (i.e. die size) is stepped, as in optical lithography across the wafer to be processed (**FIGURE 9**).

If the step-and-flash NIL technology is better suited to address the semiconductor markets (NAND flash memory, DRAM and logic) with its high level-alignment capability and its good control of defectivity density[7], the full-wafer NIL option could quickly become the reference manufacturing option for the emerging and growing markets such as LED and photonics-based devices (**FIGURE 10**).

However, this wafer-scale imprint solution still lacks quantitative data regarding its technology assessment for high-volume manufacturing. Commercial equipment[8] and resists, the cornerstones of this technology, are already available. But some links in the industrial supply chain (design rules, master manufacturing and repair, in-line defectivity and metrology controls, fully integrated process flows) still must be established and qualified to make this technology more mature.

To accelerate adoption of this technology, Leti and EV Group launched in June 2015 a new collaborative industrial program called INSPIRE, aimed at demonstrating the benefits of this full-wafer NIL technology and spreading its use for applications beyond the traditional semiconductor industry. Much more than a classic industrial partnership, the program is designed to support development of new applications from the feasibility-study stage up to the first manufacturing steps,

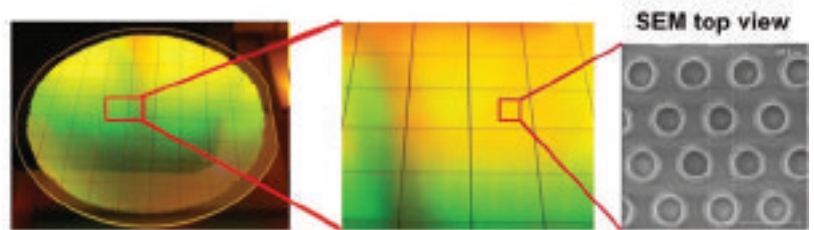


FIGURE 10. Full wafer scale imprinted wafer for photonic crystal application.

including the prototyping phase in Leti's clean room. INSPIRE is also designed to demonstrate the technology's cost-of-ownership benefits for a wide range of application domains. The final objective of this program is to facilitate the transfer of the developed integrated process solutions to industrial partners. The steps should significantly lower the entry barrier for NIL technology and speed up its use in production lines.

Conclusion

The availability of patterning alternatives in the lithography landscape represents a big opportunity to properly address the coming needs generated by the IoT. Besides conventional optical lithography, they offer industry new and/or complementary advantages: innovation capability and opportunities to better manage cost of ownership. But not only that! The high-resolution potential, the ability to facilitate design-innovation validation, and the complementarity of these alternatives with other patterning solutions also highlight their strengths. The step now is to finalize the evaluation of these technologies with respect to industry standards and establish them as real and credible lithography alternatives.

References

1. A. Schafgans et al, Proc SPIE, Extreme Ultraviolet Lithography VI, Vol. 9422, 2015
2. S. Sayan et al, Proc. SPIE, Advances in Patterning Materials and Processes XXXII, Vol. 9425, 2015
3. H. Tsai et al, ACS nano, vol 8 (5), pp. 5227-5232, 2014
4. R. Tiron et al, Alternative Lithographic Technologies II, Vol. 9423, 2015
5. L. Pain et al, SEMICON Europa symposium, Dresden, Oct 2013
6. D. Lam et al, Proc SPIE, Photomask Technology, Vol. 7823, 2010
7. H. Takeishi et al, Proc SPIE
8. EVG product flyer, EVG HERCULES NIL platform, web site: http://www.evgroup.com/en/products/lithography/nanoimprint_systems/uv_nil/hercules_nil ◀

Managing dis-aggregated data for SiP yield ramp

ED KORCZYNSKI, Senior Technical Editor

New ways are needed to feed data back and forth between designers, chip fabs, and Out-Sourced Assembly and Test (OSAT) companies.

In general, there is an accelerating trend toward System-in-Package (SiP) chip designs including Package-On-Package (POP) and 3D/2.5D-stacks where complex mechanical forces -- primarily driven by the many Coefficient of Thermal Expansion (CTE) mismatches within and between chips and packages -- influence the electrical properties of ICs. In this era, the industry needs to be able to model and control the mechanical and thermal properties of the combined chip-package, and so we need ways to feed data back and forth between designers, chip fabs, and Out-Sourced Assembly and Test (OSAT) companies. With accelerated yield ramps needed for High Volume Manufacturing (HVM) of consumer mobile products, to minimize risk of expensive Work In Progress (WIP) moving through the supply chain a lot of data needs to feed-forward and feedback.

Calvin Cheung, ASE Group Vice President of Business Development & Engineering, discussed these trends in the "Scaling the Walls of Sub-14nm Manufacturing" keynote panel discussion during the recent SEMICON West 2015. "In the old days it used to take 12-18 months to ramp yield, but the product lifetime for mobile chips today can be only 9 months," reminded Cheung. "In the old days we used to talk about ramping a few thousand chips, while today working with Qualcomm they want to ramp millions of chips quickly. From an OSAT point of view, we pride ourselves on being a virtual arm of the manufacturers and designers," said Cheung, "but as technology gets more complex and 'knowledge-base-centric' we see less release of information from foundries. We used to have larger teams in foundries." Dick James of ChipWorks details the complexity of the SiP used in the Apple Watch in his recent blog post at SemiMD, and documents the details behind the assumption that ASE is the OSAT.

With single-chip System-on-Chip (SoC) designs the 'final test' can be at the wafer-level, but with SiP based on chips from multiple vendors the 'final test' now

must happen at the package-level, and this changes the Design For Test (DFT) work flows. DRAM in a 3D stack (**FIGURE 1**) will have an interconnect test and memory Built-In Self-Test (BIST) applied from BIST resident on the logic die connected to the memory stack using Through-Silicon Vias (TSV).

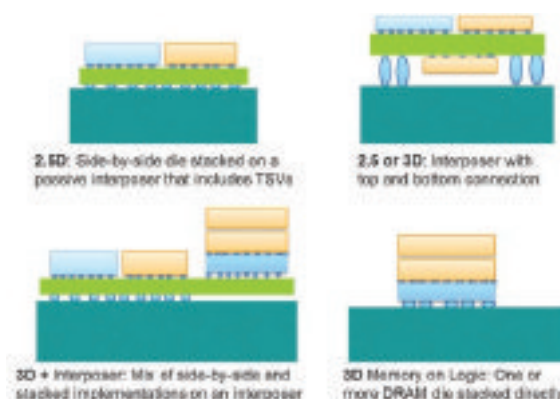


FIGURE 1. Schematic cross-sections of different 3D System-in-Package (SiP) design types (Source: Mentor Graphics).

"The test of dice in a package can mostly be just re-used die-level tests based on hierarchical pattern re-targeting which is used in many very large designs today," said Ron Press, technical marketing director of Silicon Test Solutions, Mentor Graphics, in discussion with SemiMD. "Additional interconnect tests between die would be added using boundary scans at die inputs and outputs, or an equivalent method. We put together 2.5D and 3D methodologies that are in some of the foundry reference flows. It still isn't certain if specialized tests will be required to monitor for TSV partial failures."

"Many fabless semiconductor companies today use solutions like scan test diagnosis to identify product-specific yield problems, and these solutions require a combination of test fail data and design data," explained Geir Edie, Mentor Graphics' product marketing manager of Silicon Test Solutions. "Getting data from one part of

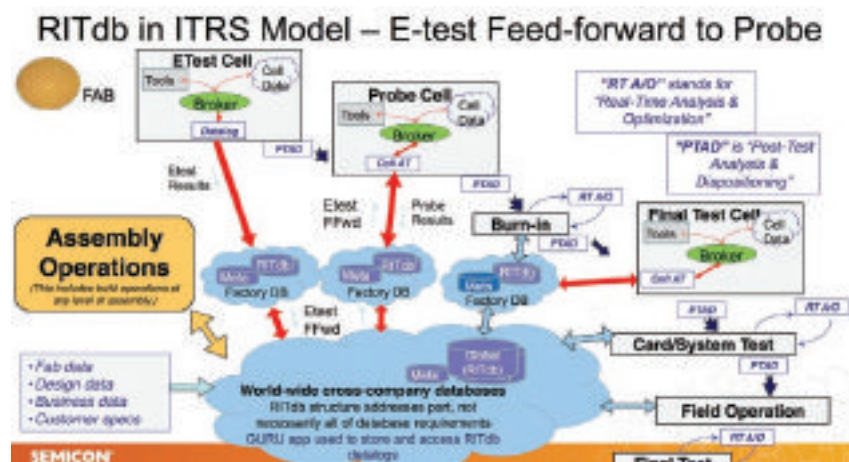


FIGURE 2. Structure of the Rich Interactive Test Database (RITdb) industry standard, showing how data can move through the supply chain (Source: Texas Instruments).

the fabless organization to another can often be more challenging than what one should expect. So, what's often needed is a set of 'best practices' that covers the entire yield learning flow across organizations."

“We do need a standard for structuring and transmitting test and operations meta-data in a timely fashion between companies in this relatively new dis-aggregated semiconductor world across Fabless, Foundry, OSAT, and OEM,” asserted John Carulli, GLOBALFOUNDRIES' deputy director of Test Development & Diagnosis, in an exclusive discussion with SemiMD. “Presently the databases are still proprietary - either internal to the company or as part of third-party vendors’ applications.” Most of the test-related vendors and users are supporting development of the new Rich Interactive Test Database (RITdb) data format to replace the Standard Test Data Format (STDF) originally developed by Teradyne.

“The collaboration across the semiconductor ecosystem placed features in RITdb that understand the end-to-end data needs including security/provenance,” explained Carulli. **FIGURE 2** shows that since RITdb is a structured data construct, any data from anywhere in the supply chain could be easily communicated, supported, and scaled regardless of OSAT or Fabless customer test program infrastructure. “If RITdb is truly adopted and some certification system can be placed around it to keep it from diverging, then it provides a standard core to transmit data with known meaning across our dis-aggregated semiconductor world. Another key part is the Test Cell Communication Standard Working Group; when integrated with RITdb, the improved automation and control path would greatly reduce manually communicated understanding of operational practices/issues across companies that impact yield and quality.”

Phil Nigh, GLOBALFOUNDRIES Senior Technical Staff, explained to SemiMD that for heterogeneous integration of different chip types the industry has on-chip temperature measurement circuits which can monitor temperature at a given time, but not necessarily identify issues cause by thermal/mechanical stresses. “During production testing, we should detect mechanical/thermal stress ‘failures’ using product testing methods such as IO leakage, chip leakage, and other chip performance measurements such as FMAX,” reminded Nigh.

Model but verify

Metrology tool supplier Nanometrics has a unique perspective on the data needs of 3D packages since the company has delivered dozens of tools for TSV metrology to the world. The company's UniFire 7900 Wafer-Scale Packaging (WSP) Metrology System uses white-light interferometry to measure critical dimensions (CD), overlay, and film thicknesses of TSV, micro-bumps, Re-Distribution Layer (RDL) structures, as well as the co-planarity of Cu bumps/pillars. Robert Fiordalice, Nanometrics' Vice President of UniFire business group, mentioned to SemiMD in an exclusive interview that new TSV structures certainly bring about new yield loss mechanisms, even if electrical tests show standard results such as 'partial open.' Fiordalice said that, "we've had a lot of pull to take our TSV metrology tool, and develop a TSV inspection tool to check every via on every wafer." TSV inspection tools are now in beta-tests at customers.

As reported at 3Dincites, Mentor Graphics showed results at DAC2015 of the use of Calibre 3DSTACK by an OSAT to create a rule file for their Fan-Out Wafer Level Package (FOWLP) process. This rule file can be used by any designer targeting this package technology at this assembly house, and checks the manufacturing constraints of the package RDL and the connectivity through the package from die-to-die and die-to-BGA. Based on package information including die order, x/y position, rotation and orientation, Calibre 3DSTACK performs checks on the interface geometries between chips connected using bumps, pillars, and TSVs. An assembly design kit provides a standardized process both chip design companies and assembly houses can use to ensure the manufacturability and performance of 3D SiP. ◀

The use of sapphire in mobile device and LED industries

WINTHROP E. BAYLIES and CHRISTOPHER JL MOORE, BayTech-Resor LLC, Maynard, MA

Sapphire is hard, strong, optically transparent and chemically inert.

Have you ever wondered what blue gemstone earrings, an LED lightbulb and an Apple Watch have in common? The answer (at least for this article) is that all depend on sapphire as part of their manufacturing process. In part 1 of the following two part article we will discuss how sapphire is becoming an important part of the mobile device food chain. Part 2 will concentrate on how sapphire is used in LED production.

Sapphire (chemical composition Al_2O_3) has a high melting point of 2040°C (3704°F) and is chemically resistant even at high temperatures. It is an anisotropic material meaning that its mechanical/thermal properties depend on the direction of the crystal plane that is cut and polished. An insulator with a 9.2 eV energy gap it is optically transparent. With a hardness of 9 on the Mohs scale it is almost as hard and strong as diamond (10 Mohs).

To summarize, sapphire has some good points: hard, strong, optically transparent and chemically inert (there is a reason high end watches use sapphire crystals) and some bad points: hard, strong, and chemically inert (which is why sapphire crystals are more expensive than glass). That is, the very properties that make it ideal for applications needing mechanical strength and hardness mean that it is a difficult material to grow, machine and polish.

There are several places where sapphire can be (or is now) used in the manufacture of mobile devices. The most publicity in this area was generated in 2014 with significant speculation in both the trade magazines and newspapers (such as the Wall Street Journal) that the iPhone 6 would be released with a sapphire touch screen or at the very least a sapphire cover glass over the existing touchscreen. Part of this speculation was fueled by the large number (1700 to 2500 depending on source) of sapphire producing furnaces being installed at an Apple facility in Mesa Arizona. However, the sapphire iPhone 6 was not released due in part to the difficulties in growing and processing enough sapphire screens at a reasonable cost to supply the significant number of phones produced. There are now sapphire touch screen phones available from other suppliers and recently, the Apple Watch was released with a sapphire screen. In addition many fingerprint sensors and camera cover glasses are now produced using sapphire as the cover material.

Requirements for sapphire material is clear (forgive the pun). For screens and cameras it must be of good optical quality i.e. transmit light well and have low surface roughness. For fingerprint sensors it needs consistent surface quality and electrical properties.



FIGURE 1. A schematic of the process used to produce sapphire parts for a mobile device.

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Production process

FIGURE 1 shows a schematic of the production process for sapphire used in a mobile device screen. The following paragraphs provide more detail on this process [1] as well as a few of problems encountered along the way.

The sapphire production process starts when a seed crystal and a mixture of aluminum oxide and crackle (un-crystallized sapphire material) is heated using a specific temperature/time profile, then cooled (this process can take two weeks depending on the amount of sapphire being produced) using a carefully controlled set of time/temperature profiles. When done correctly, the cookie sized seed grows and produces a single-crystal sapphire boule. That at least is the theory. In reality, two weeks is a long time and any number of problems can go wrong during this process including gas bubbles, mechanical faults such as cracks and contamination. Each of these problems can affect the sapphire and its optical/electrical properties. There is a clear correlation between the time taken to grow a boule and the potential quality of the boule produced. Many of the problems encountered in the upscaling of the sapphire production process sprang from trying to grow large boules at high speeds.

It is at the next step in the process where boule size does matter. Typically, the boule will be drilled or cut to produce material near the size needed for the particular application. It makes a significant difference if the material is for a watch crystal (say 1.5 inch diameter ~ 1.7 square inches). Here you can “core-drill” a boule to produce a number of smaller cylinders. For a phone screen/cover plate (at 4 by 6 inch i.e. 24 square inches) a larger portion of the boule is needed for a box shape. The ability to grow large sized boules on a regular basis is not in question; most important is how much of that boule is bubble-, crack- and impurity-free. In some cases the boules are inspected with various metrology techniques to determine which sections of the boule can be used and which cannot. The section of the boules not used is recycled into the original growth process (unless contaminated).

Given the hardness of the sapphire, diamond wire saws or diamond core drills are used for cutting or coring the boules. The yield from any boule is a function of the original boule size, the size of the cores or slabs being produced and the volume of the boule free from imper-

fections. As was discussed earlier, and is typical of many processes, the larger the size of the piece the lower the yield.

The next step is to take the cylindrical cores (or rectangular slabs) and cut them into appropriate sized pieces. The thickness of the desired part and the amount the producer is willing to invest in high technology solutions determines what is done next. On one end of the technology scale the parts are cut using a wire saw or an abrasive cutoff saw. On the other end of the scale you can ion implant the surface to produce a damaged layer at a depth below the surface determined by the original ion energy. If the slab is heated after sufficient implantation is done a thin sheet will separate from the surface. Both processes result in parts of the approximate size needed for the application; a discussion of the pros and cons of each approach is beyond the scope of this article.

The process after this point depends on the parts' final application and their manufacturer. Given the difficulty of polishing a material this hard many of the bigger companies have developed proprietary process for grinding or mechanically polishing the sapphire parts to the desired shape and surface roughness/finish. From a mechanical strength standpoint it is important that there be no significant scratching of the surface or chipping of the edges which could severely limit the mechanical strength of the final piece. From an optical standpoint it is important to produce a uniform finish



FIGURE 2. Mobile device sapphire parts partway through their production process. Figure courtesy of Chitwing-Silian.

so as not to effect the overall appearance of the part. At this stage the parts are then ground to their final size and any additional shaping of the part including holes/profiles is done. **FIGURE 2** shows a variety of sapphire parts at this stage of the process.

In most sapphire part production these parts are next coated with a variety of optical and/or electrical and/or chemical films again depending on their application. Because of its high index of refraction (1.76) a sapphire screen or watch crystal is highly reflective. For this application the parts are typically coated with a series of films to produce an anti-reflection coating enhancing final screen readability. For parts that will be touched on a regular basis such as touchscreens or fingerprint sensors coatings, it is important that they be “self-cleaning”. In these cases hydrophobic and oleophobic coatings are used to make sure your fingerprints are less likely to stay behind after the material has been touched.

FIGURE 3 shows a series of parts after the coating and silk screening process. They are now ready for assembly into the mobile device.

The use of sapphire in mobile devices is driven by two main concerns. One is that the final screen/sensor be mechanically stronger and harder than most glasses. There are a number of videos [2] available showing cement blocks being dragged over cell phones to show the sapphire screens’ scratchproof capabilities. The second (and not as well known) factor is the significant data showing that touch sensors made using sapphire have better performance characteristics due to its superior electrical properties and electrical uniformity. This allows the development of sensors which have improved performance in the field.

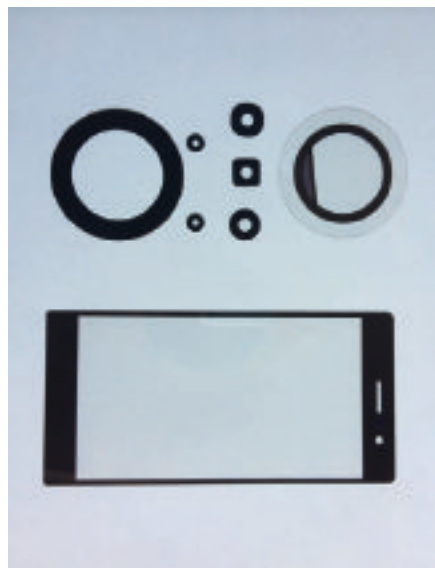


FIGURE 3. Sapphire parts after coating and inking. Figure courtesy of Chitwin-Silian.

The downside of using sapphire remains its cost. Estimates [3] have reported sapphire costs 2 to 10 times the price of an equivalent glass part. Although these costs are coming down, in price sensitive applications glass continues to dominate at this time and it is expected that only higher end phones will use sapphire screens.

In the second part of this article we will discuss the importance of sapphire in the LED industry and the difference in process needed for this material.

Additional reading/viewing material

1. <http://www.businessinsider.com/how-sapphire-glass-screens-are-made-2014-9>
2. Internet video Aero Gear's Flight Glass SX Sapphire Crystal vs a Concrete
3. <http://seekingalpha.com/article/2230553-ignore-the-sapphire-threat-corning-is-on-a-roll> ◀

Comparison of 1Ynm NAND architectures and beyond

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Expect at least two more next generation 2D planar NAND products having 12nm and less than 12nm technology.

A few years ago, some of the semiconductor process and device analysts thought 2D planar NAND Flash would soon be coming to an end due to the scaling limits, especially around the 20nm or sub-20nm generation. Do we still think the 2D NAND Flash technologies have hit the scaling wall? According to TechInsights' deep-dive analysis on current and future NAND Flash technologies, although 3D V-NAND architecture could help with the scaling limit, we believe the 2D MLC and TLC NAND Flash technologies remain strong and cost effective for 14nm, 12nm and even for single-digit nanometer node.

When it comes to 3D NAND technology, Samsung has been developing and mass-producing 32-tier V-NAND architecture with MLC and TLC for their 850 PRO and 850 EVO since 2014, although, this is not the final goal for Samsung due to a relatively low yield, process complexity and bit-cost viewpoints. More 3D Flash products may appear at the end of this year, or early in 2016, as major NAND players such

as Toshiba, SanDisk, Micron, Intel, and SK-Hynix bring out their 3D products with 24-tier, 32-tier or 48-tier FG (floating gate)/CTF (charge-trap-flash) architecture (**FIGURE 1**).

However, the ultimate target for 3D NAND is 128-tier or at least 64-tier structure from the bit-cost viewpoints. In that case, the aspect ratio of Si-channel and common source contacts would be over 80:1, which is a strong burden for process integration engineers. In addition, the uniformity of the 64-tier or 128-tier NAND cell characteristics in a NAND string and their endurance/retention/reliability properties during program/erase operation would be another big challenge for the vertical NAND string architecture.

The scaling limits for 10nm-class and sub-10nm 2D planar NAND structures include patterning technology including QPT (Quadruple Patterning Technology), cell-to-cell interference such as cross-talk, poly-Si gap-filling process for control gate (CG), self-aligned STI (SA-STI) for isolation patterning, self-aligned process (SAP) for CG/FG, interconnection methodology including pad layout/design, inter-poly dielectric (IPD) layer engineering, and cell transistor channel/source-drain (S/D) engineering. According to TechInsights' detailed structural analysis and comparison of 15nm and 16nm NAND flash devices (so called 1Y NAND technology node) such as Samsung 16nm, Toshiba 15nm, Micron 16nm and SK-Hynix 16nm products, we may expect that at least two more next generation 2D planar NAND products having 12nm; Less than 12nm technology would be developed and released from major players in the near future. As for NAND memory density and die size, Toshiba/SanDisk 15nm TLC products have 1.28 Gb/mm² which is double from other MLC products although Samsung 32-tier 3D V-NAND TLC products have 1.87 Gb/mm² (**FIGURE 2**).

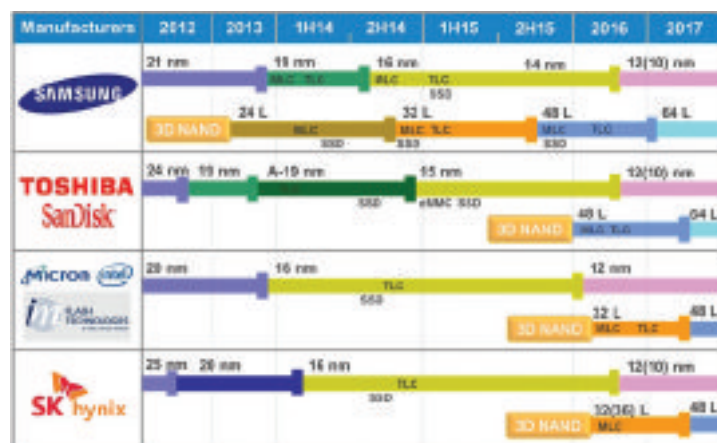


FIGURE 1. 2D and 3D NAND Technology Roadmap (Source: TechInsights Nand Roadmap).

JEONGDONG CHOE, who has more than 20 years of experience on semiconductor process and device integration including NAND Flash, DRAM, logic and advanced memory devices at Samsung and SK-Hynix, works at TechInsights as a consulting engineer especially focusing on memory and logic process integration.

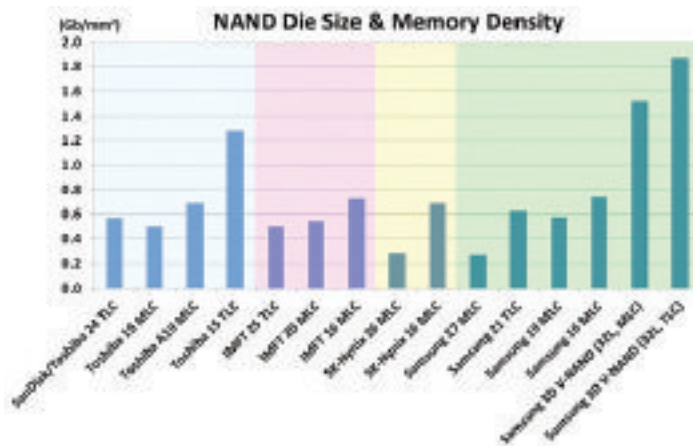


FIGURE 2. Comparison of NAND memory density for each product (Source: TechInsights).

For patterning the three finest lines of the NAND cell structure such as active/STI, gate/wordline (CG/FG) and bitline (usually, metal-2 lines), a quadruple patterning technology (QPT) seems to be very mature for each of the major NAND players. They use their own QPT integration on three critical layers with three or four masks, SOH etching and two-step self-align reverse patterning (SARP) process. Although the critical dimensions have a little skew on every four patterns, they have successfully developed QPT integration with less than 1nm CD (Critical Dimension) and it could be extended into 10nm and even single-digit nanometer NAND products. Fortunately and thanks to state-of-the-art anisotropic plasma etching and ALD/CVD technology, uniformly repeated 8nm patterns would be possible for NAND cell array. **FIGURE 3** shows a comparison of DPT/QPT patterns for each product.

Micron uses a 3.3nm thin-FG poly-Si storage node to decrease cell-to-cell interference, while other manufacturers introduce an air-gap process for active, gate wordline (FG/CG) and bitline (metal-2) for thick-FG structure. Especially, the air-gap process has been developed and applied on the channel region of active patterns and FG/CG pillars help decrease the cross-talk.

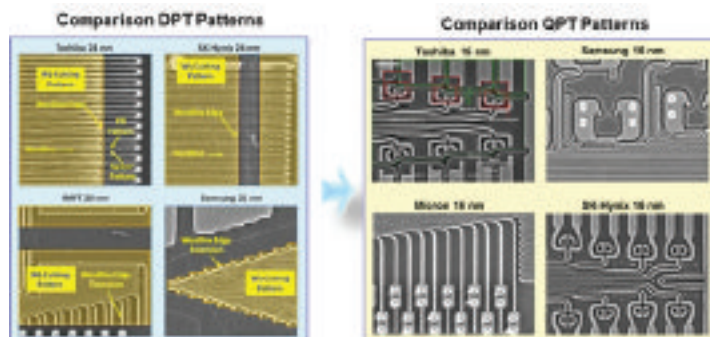


FIGURE 3. Comparison of DPT and QPT patterns for each product (Source: TechInsights).

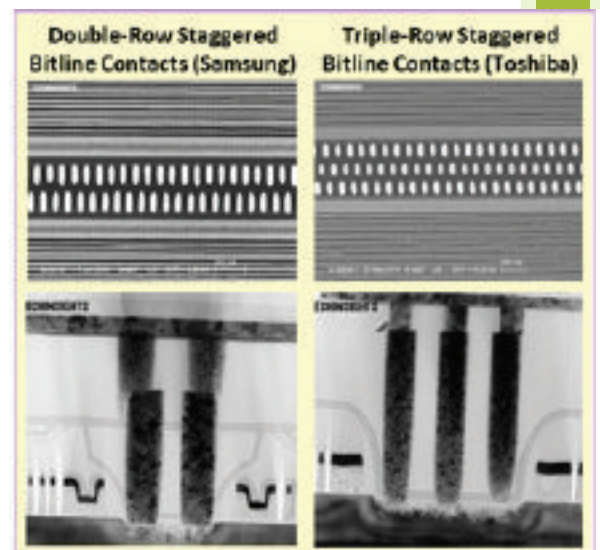


FIGURE 4. Double- and triple-row staggered bitline contacts (Source: TechInsights).

For an IPD (Inter-Poly Dielectric) or a barrier layer between CG and FG, a multi-layer stacked with thin oxide and nitride layers such as ONO or NONON structure has been used for mid-10nm class NAND devices, while Micron uses a high-k dielectrics such as HfO/SiO/HfO/Nitrided-SiO which is the same as their 20nm NAND products. Micron successfully integrated IPD/FG/Tunnel-oxide and decreased FG thickness from 5nm to 3.3nm with high-k IPD. It might be further reduced to 10ish nm NAND products by optimizing IPD/FG quantum well structure for their unique thin-FG architecture. A 6nm tunnel oxide (SiO₂) is used on Micron, Toshiba/SanDisk and SK-Hynix, while Samsung uses nitrogen-doped oxide in its top and bottom portion.

Triple-row staggered bitline contacts (BC) are used on Toshiba/SanDisk for the first time which is an excellent choice to make things smooth for cell layout and process integration although NAND string overhead is increased from 13% to 19%. Other players still use double-row staggered BC layouts on their 15nm/16nm NAND products (**FIGURE 4**).

Other barriers to extend 2D planar NAND to 10nm such as CG poly fill-ability, anisotropic etching for SA-FG/STI and CG/FG, cell transistor S/D engineering and leaning effect during the process integration are still there. Nevertheless, major players and their equipment vendors will successfully develop and integrate the 10nm 2D NAND architecture in a few years.

I believe most of the major NAND players have their own matured process integration capability with assistance from ECC and circuit/layout optimization. 2D NAND technology will be further scaled down to 12nm, 10nm, or even 8ish nm which is more cost-effective than 3D V-NAND for near future NAND products. ♦



Time is the enemy of profitability

DOUGLAS G. SUTHERLAND and **DAVID W. PRICE**, KLA-Tencor, Milpitas, CA

Time is a critical element in all phases of semiconductor manufacturing.

In previous installments we discussed capability, sampling, missed excursions, risk management and variability. Although all of these topics involve an element of time, in this paper we will discuss the importance of timeliness in more detail.

The sixth fundamental truth of process control for the semiconductor IC industry is:

Time is the Enemy of Profitability

There are three main phases to semiconductor manufacturing: research and development (R&D), ramp, and high volume manufacturing (HVM). All of them are expensive and time is a critical element in all three phases.

From a cash-flow perspective, R&D is the most difficult phase: the fab is spending hundreds of thousands of dollars every day on man power and capital equipment with no revenue from the newly developed products to offset that expense. In the ramp phase the fab starts to generate some revenue early on, but the yield and volume are still too low to offset the production costs. Furthermore, this revenue doesn't even begin to offset the cost of R&D. It is usually not until the early stages of HVM that the fab has sufficient wafer starts and sufficient yield to start recovering the costs of the first two phases and begin making a profit. **FIGURE 1** shows the cumulative cash flow for the entire process.

What makes all of this even more challenging is that all the while, the prices paid for these new devices are falling. The time required from

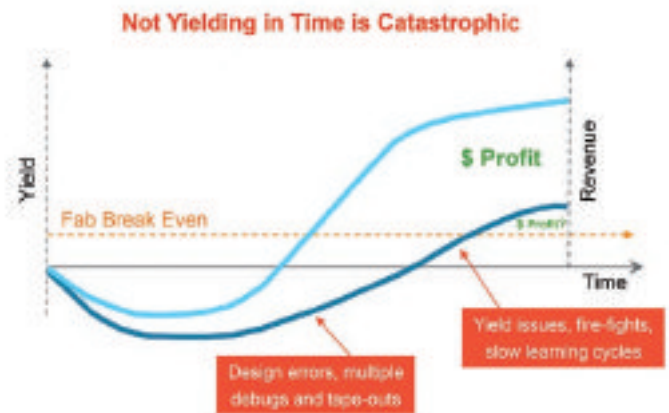


FIGURE 1. The cumulative cash-flow as a function of time. In the R&D phase the cash-flow is negative but the slope of the curve turns positive in the ramp phase as revenues begin to build. The total costs do not turn positive until the beginning of high-volume manufacturing.

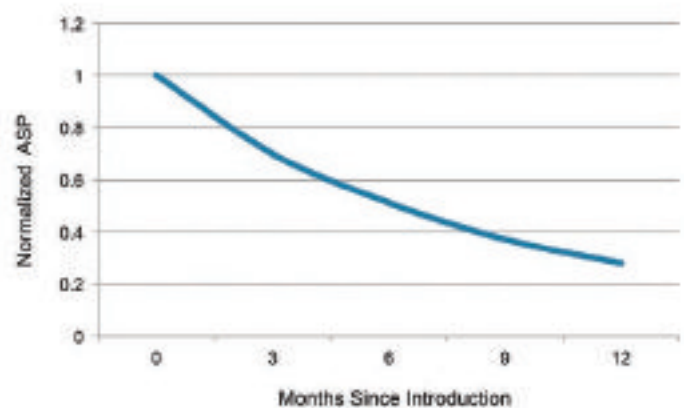


FIGURE 2. Typical price decline curve for memory products in the first year after product introduction. Similar trends can be seen for other devices types.

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initial design to when the first chips reach the market is a critical parameter in the fab's profitability. **FIGURE 2** shows the actual decay curve for the average selling price (ASP) of memory chips from inception to maturity.

Consequently, while the fab is bleeding money on R&D, their ability to recoup those expenses is dwindling as the ASP steadily declines. Anything that can shorten the R&D and ramp phases shortens the time-to-market and allows fabs to realize the higher ASP shown on the left hand side of Figure 2.

From Figures 1 and 2 it is clear that even small delays in completing the R&D or ramp phases can make the difference between a fab that is wildly profitable and one that struggles just to break even. Those organizations that are the first to bring the latest technology to market reap the majority of the reward. This gives them a huge head start—in terms of both time and money—in the development of the next technology node and the whole cycle then repeats itself.

Process control is like a window that allows you to see what is happening at various stages of the manufacturing cycle. Without this, the entire exercise from R&D to HVM would be like trying to build a watch while wearing a blindfold. This analogy is not as far-fetched as it may seem. The features of integrated circuits are far too small to be seen and even when inspections are made, they are usually only done on a small percentage of the total wafers produced. For parametric measurements (films, CD and overlay) measurements are performed only on an infinitesimal percentage of the total transistors on each of the selected wafers. For the vast majority of time, the fab manager truly is blind. Parametric measurements and defect inspection are brief moments when 'the watch maker' can take off the blindfold, see the fruits of their labor and make whatever corrections may be required.

As manufacturing processes become more complex with multiple patterning, pitch splitting and other advanced patterning techniques, the risk of not yielding in a timely fashion is higher than ever. Having more process control steps early in the R&D

and ramp phases increases the number of windows through which you can see how the process is performing. Investing in the highest quality process control tools improves the quality of these windows. A window that distorts the view—an inspection tool with poor capture rate or a parametric tool with poor accuracy—may be worse than no window at all because it wastes time and may provide misleading data. An effective process control strategy, consisting of the right tools, the right recipes and the right sampling all at the right steps, can significantly reduce the R&D and ramp times.

On a per wafer basis, the amount of process control should be highest in the R&D phase when the yield is near zero and there are more problems to catch and correct. Resolving a single rate-limiting issue in this phase with two fewer cycles of learning—approximately one month—can pay for a significant portion of the total budget spent on process control.

After R&D, the ramp phase is the next most important stage requiring focused attention with very high sampling rates. It's imperative that the yield be increased to profitable levels as quickly as possible and you can't do this while blindfolded.

Finally, in the HVM phase an effective process control strategy minimizes risk by discovering yield limiting problems (excursions) in a timely manner.

It's all about time, as time is money.

References

1. Process Watch: You Can't Fix What You Can't Find, Solid State Technology, July 2014
2. Process Watch: Sampling Matters, Semiconductor Manufacturing and Design, September 2014
3. Process Watch: The Most Expensive Defect, Solid State Technology, December 2014
4. Process Watch: Fab Managers Don't Like Surprises, Solid State Technology, December 2014
5. Process Watch: Know Your Enemy, Solid State Technology, March 2015 ♦

Cut costs: Improve Competitive Advantage.

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Systematic – and predictive – cost reduction in semiconductor equipment manufacturing

After a period of double-digit growth, the semiconductor equipment industry has now stabilized to the point where recent market forecasts are predicting anemic single-digit growth rates. This is driven by total market demand from chipmakers. For example, despite strong growth of 12.9 percent in 2014, Gartner, Inc. projects worldwide semiconductor capital spending to only grow 0.8 percent in 2015, to \$65.7 billion. [1] Additionally, this industry has always been subject to volatile demand cycles that are notoriously difficult to predict.

Translation: It's extremely challenging for today's semiconductor equipment manufacturers to improve their financial performance. There are fewer and fewer opportunities to grow topline revenue through innovation and new product development. And, after several years of cutting costs on existing products and not realizing enough cost reduction to improve margins, it's difficult to know how to do it differently.

Yet a viable alternative to improve financial performance does exist: A disciplined, rigorous, and systematic approach to reducing costs that delivers more predictive results.

A systematic approach to cost reduction

Where cutting costs was once perceived as the end result of "desperate times, desperate measures," many innovators are now using this approach much more proactively. By meeting the idea of cost reduction head on – as an opportunity, not a last resort – many semiconductor equipment makers are uncovering wasteful, inefficient, and costly processes, often in areas they once overlooked.

At this point, you may be thinking, "All of this sounds great, but what is a systematic approach to cost reduction, and how is it different from what I'm doing?"

Remember that many manufacturers (in all industries) tend to have a hard time driving costs down. They may set cost reduction goals and then attempt to achieve them using various ad hoc approaches. But they really need to understand exactly what their true costs are, where they exist, and which areas will improve their margins.

A systematic approach to cost reduction gives them this insight. With improved visibility into the entire organization, various processes, and how they execute, semiconductor equipment manufacturers can't identify the right places to cut costs and hit their cost savings goals. This is a very detailed and planned approach in which organizations closely examine areas such as cost of goods sold, R&D, and service to make more informed decisions that will position their business for long-term success. This is the value of a systematic approach to cost reduction.

This approach also introduces the element of speed, helping equipment makers realize cost savings much faster than ad hoc cost-cutting initiatives and puts them on a path to achieve more predictive results. Beyond the positive (and more obvious) impact successful cost reduction has on a semiconductor equipment manufacturer's bottom line, it also provides a number of significant benefits such as improving productivity, freeing up key personnel, and providing needed capital to fuel new growth.

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The path to predictive results

Even if the concept of a more strategic approach to cutting costs sounds reasonable, many semiconductor equipment manufacturers struggle with how to begin and where to focus. All too often they resort to making reactive decisions regarding existing products without the necessary data, leading them to ask questions such as, “Should we have an obsolescence plan for this product?” “How much could we save?” and “Will this lead to bigger problems down the road?”

Without understanding where your best opportunities for cost cutting are, it's a lot harder to predict when, and if, cost reduction goals will be met. A systematic approach to cost reduction includes establishing clear cost targets, communicating them to leadership, and measuring and reporting results along the way.

The first step is to engage with an outside firm that has a singular focus on cost reduction, and one that is clearly separated from day-to-day operations and current organizational dynamics. Such an engagement will yield an actionable list of improvements with specific cost targets, realistic timelines for achieving these goals, and future plans for reinvesting the cost savings.

More specifically, a systematic cost reduction approach will focus on three key areas: material costs, R&D costs, and service costs:

1. Material costs: The bill of materials is one of the most common ways to see all the components needed to produce the end product. But this goes well beyond the pure cost of materials. Research has shown that improving the way these components are managed can affect 80-90% of the product's total costs.[2]

For semiconductor equipment manufacturers, the cost reduction process should start with the selection of the products or sub-assemblies that have the highest potential for savings. Focus on those products that are still generating significant revenue, but may not be receiving much attention in terms of engineering upgrades and enhancements. Thoroughly examine the bill of materials for these products by addressing materials, design, complexity reduction, the potential to create common assemblies, and more.

Value engineering efforts can simultaneously improve product functionality and performance while reducing bill of material costs. This effort should factor in ways to meet RoHS requirements and when to make end-of-life decisions for various electrical components to improve

design efficiency and the effectiveness of the product.

A realistic cost reduction goal can then be created and a resulting value-engineering project can commence, often using low-cost offshore resources to best achieve those savings.

2. R&D costs: Making better decisions related to R&D processes and product development can shave considerable costs. Some areas to focus on include:

- When to officially end of life non-performing products
- When to consolidate products, or possibly even entire R&D departments
- When and how to move sustaining engineering efforts offshore, or to other lower-cost alternatives

The critical next step is to look at all products and all product variations to determine if an official end-of-life program should be employed. These decisions are notoriously hard to make and often require difficult conversations with key customers, but they are necessary nonetheless.

Many semiconductor equipment manufacturers have grown through acquisitions, creating redundant engineering groups that can be eliminated or downsized. Performing an organizational analysis of all R&D activities may uncover opportunities to consolidate and combine functions or create centers of excellence that focus on specific technical areas eliminating redundancies of technical specialty.

3. Service costs: Examine engineering and design processes to find ways to improve performance, reliability, and costs. For example, adding data collection technology or product diagnostics to enhance remote support efforts and predictive maintenance.

Improvement of product reliability is usually a large multiplier when it comes to service and spare parts costs. Collect and analyze field data to find the most significant issues driving service costs and then look to cut where possible.

For example, equipment in the field often does not have the capability to report enough information to effectively identify a problem. Adding increased data logging and communication can be used to clarify machine status and point services in the right direction. Connectivity can also help with remote diagnostics, all of which helps reduce costs, uptime, and customer satisfaction.

Cost Reduction as a Competitive Advantage

Short-term market forecasts will continue to make it challenging for semiconductor equipment manufacturers to deliver improved financial results. Yet the concept of a systematic approach to cost reduction is a proven way for them to proactively cut costs – in the right places – and also make better decisions related to existing products and other business systems and processes.

By taking a disciplined, rigorous, and objective look at any and all parts of their organization, semiconductor equipment makers can capitalize on new opportunities to free valuable resources, improve processes and future technology, and reinvest savings for future growth. For many equipment manufacturers the greatest obstacle to successfully exploiting these opportunities is insufficient experience and expertise with a disciplined and unconventional way of approaching cost reduction projects. A systematic approach to cost reduction will be the key to success for companies looking to improve their competitive advantage.

References

1. Gartner, Inc., "Gartner Says Worldwide Semiconductor Capital Spending to Increase 0.8 Percent in 2015: Conservative Investment Strategies Paving the Way to Slower Growth in 2015," January 13, 2015. <http://www.gartner.com/newsroom/id/2961017>.
2. Forbes, "Product Lifecycle Management: A New Path to Shareholder Value?" August 5, 2011, <http://www.forbes.com/sites/ciocentral/2011/08/05/product-lifecycle-management-a-new-path-to-shareholder-value/>. ◀

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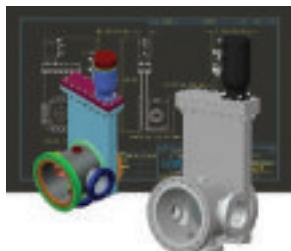
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Update for exporters: Trade wins and delays

With trade policy dominating headlines in recent weeks, all eyes were on Maui in the waning days of August as trade ministers from twelve nations convened for perhaps the final time to finalize the Trans-Pacific Partnership (TPP). Such a pact between Pacific Rim economies would account for 40% of the world's GDP. However, last-minute hurdles on dairy, autos, and drug provisions proved to be the negotiators' undoing and ministers left Hawaii with the promise of at least one more round of exhaustive deliberations in the fall.

Such is the pathway for a multilateral agreement like the TPP. By all accounts, significant progress has been made but getting 12 countries to concur on a high-standard agreement to reduce both tariffs and non-tariff barriers has been arduous to say the least. The business community remains optimistic nonetheless and will continue to support TPP conclusion—key for the U.S. SEM industries which export 80% of their products—later this year.

Conversely, a sector-specific trade agreement is a bit more straightforward and industry welcomed news just a week earlier that an agreement-in-principle was reached on the expansion of the Information Technology Agreement (ITA). Originally agreed to in 1996, the ITA fosters free trade in tech and has sorely needed an update to account for the vast progress made through industrial innovation. While this effort was not without its own obstacles, World Trade Organization (WTO) members came to an agreement in Geneva on July 24th to cut tariffs on more than 200 ICT products after more than three years of negotiations.

This deal between more than 50 nations is seen a major victory for the global economy and the semiconductor equipment and materials industries in particular. SEM-related items account of more than a dozen of the products on the expansion list, including machines and apparatus to manufacture boules, wafers, semiconductor devices and flat panel displays among other products of interest to SEMI members.



WTO trade ministers will now take the list back to their respective capitals for domestic consultations. By November 1st, participating members

TAYLOR SHOLLER, SEMI

must submit a draft schedule detailing their plans for national implementation. The process should culminate during the WTO's 10th Ministerial Conference in Nairobi in December 2015, with tariff elimination slated to begin July 2016.

The expanded agreement represents 97% of world trade in information technology products—an estimated \$1.3 billion annual market. However, the deal also contains a commitment to work to tackle non-tariff barriers in the IT sector, and to keep the list of products covered under review to determine whether further expansion may be needed to reflect future technological developments.

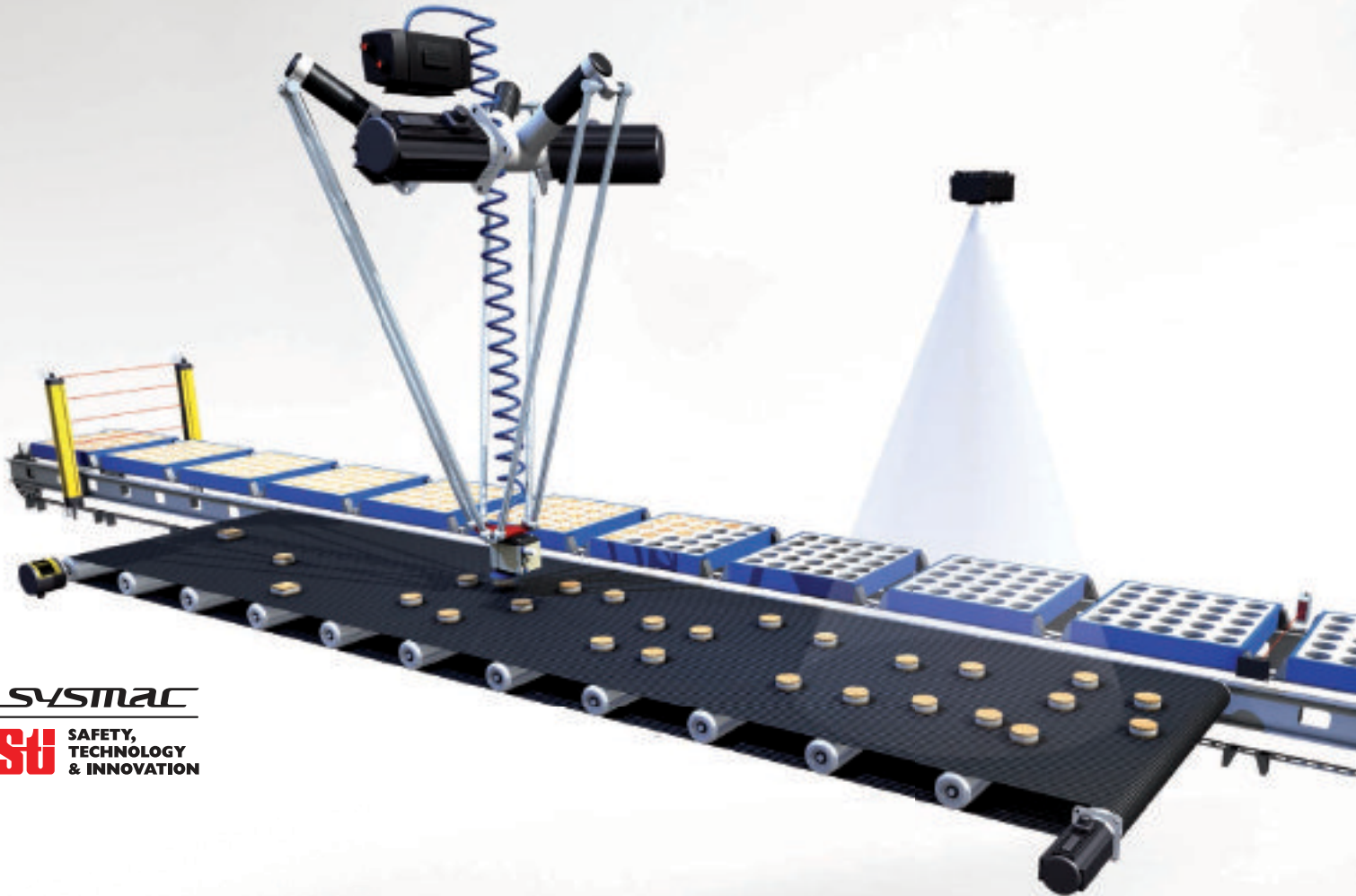
In what was already been a successful year for trade liberalization, negotiators should soon celebrate implementation of the largest WTO-driven tariff elimination deal in 19 years. The process has breathed fresh life into the promise of sectoral trade pacts driven by market demand and targeted negotiations. SEMI has worked closely with ITA negotiators throughout the process to ensure the inclusion of SEM items in the expanded list and this is something we hope to replicate in other market opening accords like the Environmental Goods Agreement as well.

The semiconductor supply chain is comprised of the most innovation and technologically advanced products in the world and trade agreements like the ITA play an exceedingly helpful role in the advancement of our industry. WTO Director-General Roberto Azevedo and trade negotiators around the world should be commended for their persistence on this important expansion effort. SEMI will continue to support the great work happening in Geneva and elsewhere to remove barriers to trade and improve business operations for our members.

For a complete list of items included in the expanded ITA, please visit: <https://ustr.gov/sites/default/files/ITA-expansion-product-list-2015.pdf>

For those with trade-specific questions or concerns, SEMI maintains a dedicated international policy staff, led by Jonathan Davis, Global Vice President of Advocacy (jdavis@semi.org). <◆

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