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SEPTEMBER 2014

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Insights for Electronics Manufacturing

Lithography: What are the alternatives to EUV?

P. 14

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Solid State TECHNOLOGY

SEPTEMBER 2014 VOL. 57 NO.6

The Applied Producer XP Precision CVD system solves the demanding, fundamental deposition challenges presented by vertical 3D NAND architectures.

COVER

FEATURES

COLUMNS

DEPARTMENTS

Web Exclusives

The 10 fundamental truths of process control for the semiconductor IC industry

This is the first in a series of 10 installments which will discuss fundamental truths about process control—inspection and metrology—for the semiconductor industry. Each article in this series will introduce one of the 10 fundamental truths and discuss interesting applications of these truths to semiconductor IC fabs.

http://bit.ly/1sSYuMT

CEA-Leti: Monolithic 3D is the solution for further scaling

Hughes Metras, Leti's VP of Strategic Partnerships North America, introduced the lead talk at their SemiconWest 2014 Leti Day about monolithic 3D technology as the "solution for scaling." Hughes presented the Leti device technology roadmap which showed monolithic 3D (M3D) as an alternative to scaling from the 2Xnm nodes to well past 5nm.

http://bit.ly/VjulWw

Paradigm shift in semi equipment – Confirmed

Our blog Paradigm shift: Semi equipment tells the future, was focused on the quote: "Now more money is spent on upgrading existing facilities, while new capacity additions are occurring at a lower pace." And now, just prior to Semicon West, we have the conclusion of the recent SEMI's World Fab Forecast — Technology Node Transitions Slowing Below 32 nm.

http://bit.ly/1rreaG5

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http://bcove.me/3hzx2ei7

n&b news and blogs

New benchmark for EUV established

Vivek Bakshi of EUV Litho, Inc. blogs on a recent watershed moment for EUV as it establishes the benchmark capability of the EUV source and scanner to support semiconductor technology node development.

http://bit.ly/Y4F0vr

TSMC 20nm arrives –The first shoe drops

2014 so far has been the year of waiting for parts and processes that have been announced, but not shown up in the world of commercial production. Dick James, Senior Technology Analyst, unwraps a TSMC-fabbed 20nm part in this recent blog post.

http://bit.ly/VjljOJ

Insights from the Leading Edge: The drama continues in IBM/GlobalFoundries deal

Contributing Editor Dr. Phil Garrou discusses the recent reports on potential consolidation.

http://bit.ly/1oJmii8

The changing face of semiconductor investment

Innovation is alive and well in the semiconductor industry. That was a key takeaway from the strategic investor panel at the second annual Silicon Innovation Forum at SEMICON West, and one I can't reinforce enough within the venture capital (VC) community. *(From SemiMD, part of the Solid State Technology network)*

http://bit.ly/1sVpTQp

editorial

Beautiful, brilliant people

It would be difficult to overstate how critical the development of a workable, high volume manufacturing EUV lithography solution is to the semiconductor industry. It is no doubt why Intel, TSMC and Samsung invested billions in ASML in 2012, and why ASML acquired Cymer in 2013.

Progress has been slower than hoped, and many are questioning if it will be ready for the 10nm generation, which is slated to go into production in late 2015/early 2016. The cover story this month looks at alternatives, including mutli e-beam and directed self-assembly.

> "A thousand people at Cymer spend their life trying to make this work."

A push to 3D devices, such as the vertical NAND, make continued scaling possible while lessening the lithography (although new challenges are created for deposition and etch technologies).

The good news is that it's possible to get to 10nm and even 7nm without EUV using multi-patterning. The only question is if it will be cost effective to do so.

Earlier this year, at the SEMI Northeast Forum held in Billerica, MA, Patrick Martin, Senior Technology Director at Applied Materials described EUV as a "huge challenge" but then noted that "beautiful, brilliant people are working on this. He said "a thousand people at Cymer spend their life trying to make this work."

I thought this was an interesting insight. It's too easy to only look at the myriad of technology challenges that exist in something complex as EUV and think it's not workable. But if we consider the human factor and that so many people are dedicating their lives to make it work (not to mention the billions of dollars at stake), it suddenly seems very achievable.

One EUV proponent is our blogger Vivek Bakshi, who runs regular workshops on EUV. In August, he reported on some recent good news announced by IBM showing good results using the ASML EUV tool at the Albany Nanotech center (summarized in this issue on pg. 13). What was a little sad was how many negative comments were made. I suppose with something as critically important as EUV, it's to be expected that emotions will run high. But let's not forget those beautiful, brilliant people that are spending their days trying to make it work.

—Pete Singer, Editor-in-Chief

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USA | **SRC** and **UC Davis** released research on next-generation materials and device structures to develop "Race Track Memory" technologies.

ASIA | **Semiconductor Manufacturing International Corporation** and **Jiangsu Changjiang Electronics Technology Co., Ltd.** jointly announced the formation of a joint venture for 12-inch bumping and related testing.

USA | **Nordson** completed its acquisition of Avalon Laboratories.

ASIA | **New Japan Radio Co., Ltd.** and **United Microelectronics Corporation** announced that the two companies have successfully collaborated to achieve high-volume manufacturing for NJR's MEMS microphone products.

USA | **Quantum Materials** achieved 95% quantum yield by automated quantum dot production.

EUROPE | **Cambridge Nanotherm** appointed Ralph Weir as CEO.

USA | **The Facilities 450mm Consortium** (F450C) announced it has again increased in size, naming **Pfeiffer Vacuum** as the twelfth member company to join the consortium.

ASIA | **A*STAR's Institute of Microelectronics**, along with 10 industry partners, launched four join laboratories. The industry partners involved in this international collaboration are: **Applied Materials, Dai Nippon Printing, DISCO, KLA-Tencor, Mentor Graphics, Nikon, Panasonic Factory Solutions Asia Pacific, PINK, Tokyo Electron Ltd. and Tokyo Ohka Kogyo.**

Strong growth in second quarter 2014 silicon wafer shipments

Worldwide silicon wafer area shipments increased during the second quarter 2014 when compared to first quarter area shipments according to the SEMI Silicon Manufacturers Group (SMG) in its quarterly analysis of the silicon wafer industry.

Total silicon wafer area shipments were 2,587 million square inches during the most recent quarter, a 9.5 percent increase from the 2,363 million square inches shipped during the previous quarter. New quarterly total area shipments are 8.2 percent higher than second quarter 2013 shipments.

"For two consecutive quarters, strong silicon shipment growth has been recorded by the Silicon Manufacturers Group," said Hiroshi Sumiya, chairman of SEMI SMG and general manager of the Corporate Planning Department of Shin-Etsu Handotai Co., Ltd. "Silicon wafer shipments reached an all-time high in the second quarter, surpassing the previous peak of 2,489 million square inches shipped in the third quarter of 2010."

Silicon wafers are the fundamental building material for semiconductors, which in turn, are vital components of virtually all electronics goods, including computers,

Continued on page 8

Global semiconductor industry on pace for record sales through first half of 2014

The Semiconductor Industry Association (SIA) today announced that worldwide sales of semiconductors reached $82.7 billion during the second quarter of 2014, an increase of 5.4 percent over the previous quarter and a jump of 10.8 percent compared to the second quarter of 2013. Global sales for the month of June 2014 reached $27.57 billion, marking the industry's highest monthly sales ever. June's sales were 10.8 percent higher than the June 2013 total of $24.88 billion and 2.6 percent more than last month's total of $26.86 billion. Year-to-date sales during the first half of 2014 were 11.1 percent higher than they were at the same point in 2013, which was a record year for semiconductor revenues. All monthly sales numbers are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average.

"Through the first half of 2014, the global semiconductor market has demonstrated consistent, across-the-board growth, with the Americas region continuing to show particular strength," said Brian Toohey, president and CEO, Semiconductor Industry Association. "The industry posted its highest-ever second quarter sales and outperformed the

Continued on page 8

SEMATECH and CNSE/SUNY launch new patterning center

SEMATECH and the newly merged SUNY College of Nanoscale Science and Engineering (CNSE) / SUNY Institute of Technology (SUNYIT) announced they have launched their joint Patterning Center of Excellence. The new Center will leverage the CNSE/SUNYIT lithography infrastructure which includes film deposition and etch capability, leading-edge patterning systems and SEMATECH's Resist Materials Development Center's (RMDC) EUV imaging capabilities.

Continued on page 9

Solid State Technology and SEMI announce the 2014 "Best of West" Award winner

At SEMICON West 2014, Solid State Technology and SEMI announced the recipient of the 2014 "Best of West" Award — Nikon Corporation — for its NSR-S630D Immersion Scanner. The award recognizes important product and technology developments in the microelectronics supply chain. The Best of West finalists were selected based on their financial impact on the industry, engineering or scientific achievement, and/or societal impact.

Continued on page 10

Continued from page 6

QUARTERLY SILICON AREA SHIPMENT TRENDS

	Millions Square Inches		
	Q2 2013	Q1 2014	Q2 2014
Total	2,390	2,363	2,587
Market	Last Month	Current Month	% Change

telecommunications products, and consumer electronics. The highly engineered thin round disks are produced in various diameters (from one inch to 12 inches) and serve as the substrate material on which most semiconductor devices or "chips" are fabricated.

All data cited in this release is inclusive of polished silicon wafers, including virgin test wafers, epitaxial silicon wafers, and non-polished silicon wafers shipped by the wafer manufacturers to the end-users.

The Silicon Manufacturers Group acts as an independent special interest group within the SEMI structure and is open to SEMI members involved in manufacturing polycrystalline silicon, monocrystalline silicon or silicon wafers (e.g., as cut, polished, epi, etc.). The purpose of the group is to facilitate collective efforts on issues related to the silicon industry including the development of market information and statistics about the silicon industry and the semiconductor market.

Continued from page 6

latest World Semiconductor Trade Statistics (WSTS) sales forecast. Looking forward, macroeconomic indicators – including solid U.S. GDP growth announced last week – bode well for continued growth in the second half of 2014 and beyond."

Regionally, sales were up compared to last month in the Americas (4.9 percent), Asia Pacific (2.1 percent), Japan (2.1 percent), and Europe (1.9 percent). Compared to June 2013, sales increased in the Americas (12.1 percent), Europe (12.1 percent), Asia Pacific (10.5 percent), and Japan (8.5 percent). All four regional markets have posted better year-to-date sales through the first half of 2014 than they did through the same point last year.

June 2014			
Billions			
Month-to-Month Sales			
Market	Last Month	Current Month	% Change
Americas	5.09	5.34	4.9%
Europe	3.13	3.19	1.9%
Japan	2.89	2.95	2.1%
Asia Pacific	15.76	16.09	2.1%
Total	**26.86**	**27.57**	**2.6%**
Year-to-Year Sales			
Market	Last Year	Current Month	% Change
Americas	4.76	5.34	12.1%
Europe	2.84	3.19	12.1%
Japan	2.72	2.95	8.5%
Asia Pacific	**14.56**	**16.09**	**10.5%**
Total	**24.88**	**27.57**	**10.8%**
Three-Month-Moving Average Sales			
Market	Jan/Feb/Mar	Apr/May/June	% Change
Americas	5.08	5.34	5.1%
Europe	3.08	3.19	3.5%
Japan	2.81	2.95	4.9%
Asia Pacific	15.18	16.09	6.0%
Total	26.15	27.57	5.4%

Continued from page 7

The Patterning Center of Excellence (CoE) will enable lithography equipment and lithographic materials manufacturing companies access to a vertically integrated semiconductor processing facility. The new Center aims to reduce the tangible and intangible costs of developing critical lithography materials for individual semiconductor companies. CNSE has continued to build capability, enabling technological excellence as represented by the Center for Semiconductor Research (CSR), a leading-edge research center valued at more than $1 billion established at CNSE in May 2005; the Global 450 Consortium (G450C), which is focused on building the 450mm wafer and equipment development environment; and by CNSE's membership in SEMATECH.

"Building on SEMATECH's recent achievements in mask blank and resist, the new Patterning Center will provide the critical capabilities that will continue to produce the results that our members and the industry need to show that EUV lithography is manufacturable," said Michael Lercel Senior Director and Chief Technologist at SEMATECH. "Furthermore, the new Center will provide an excellent platform for advancing cost-effective semiconductor materials and process solutions needed to enable EUV and emerging patterning technologies."

"The new Patterning Center further builds on the world-class capabilities enabled by the SEMATECH-CNSE/SUNYIT partnership to support the commercialization of EUVL technologies," said Dr. Michael Liehr, Executive Vice President of Innovation and Technology of the newly merged CNSE/SUNYIT. "New York State continues to chart a pioneering path for the semiconductor industry under the leadership of Governor Andrew Cuomo, and we are delighted to support the advanced technology needs of our global corporate partners and the industry."

Advances in lithographic patterning critically depend on the timely availability of enabling resists and materials. The new center, a vital component that builds on SEMATECH's mask blank and novel imaging efforts, will enable companies to assess their materials, test new tooling, and validate designs for the manufacturing EUVL and other next-generation technologies through access to the newly merged CNSE/SUNYIT's advanced fabrication facilities.

"The challenges for advanced lithography are developing resist processes that meet the stringent resolution, linewidth roughness, and sensitivity specifications," said Kevin Cummings, SEMATECH's Director of Lithography. "These processes will not be available in time without intervention, and the Patterning Center is the place where the industry's the most advanced technologists can come together and partner to commercialize extreme ultraviolet (EUV) lithography and other technologies for the manufacturing of future nanoelectronics devices."

"The industry is at a crossroads," said Warren Montgomery, Assistant Vice President of Advanced Technology and Business Development at the newly merged CNSE/SUNYIT. "The high cost of R&D has made it very difficult to do the research and development needed to continue the drive to smaller and smaller features sizes. The creation of collaborative 'centers' like the Centers of Excellence at CNSE and this newly created Patterning Center, being created by CNSE and SEMATECH,

Continued on page 10

Continued from page 9

will enable R&D to continue while keeping the economics reasonable."

"SEMATECH remains committed to finding cost-effective solutions through its connections with a broad base of member company engineers, suppliers, and academic researchers to ensure the affordable evolution of emerging lithography technologies," said Edward Barth Director of Strategic Growth Initiatives at SEMATECH. "Building on SEMATECH's latest development efforts in mask and novel imaging, the new Center will provide an excellent platform for advancing cost-effective semiconductor materials and process solutions for future nanoelectronics devices."

Over the past decade, SEMATECH has enabled fast cycle time of resist and materials development by providing the industry access to successive generations of small field exposure tools. In addition, SEMATECH's projects have succeeded in measuring the outgassing characteristics in hundreds of EUV resists and materials formulations, and delivering thousands of EUV exposure shifts to member companies that have enabled tens of thousands of materials formulations to be evaluated.

CNSE/SUNYIT has, over the past decade, enabled advanced 193nm resist and materials development, etch characterization, defect characterization and integrated process flow demonstration to its partner ecosystem.

SEMATECH and CNSE/SUNYIT's new Patterning Center is taking the collaboration with CNSE/SUNY IT and its global ecosystem and research network one step further by enabling them to share the costs for advancing resist and materials and process development to support the critical needs of industry. ◆

Continued from page 7

Nikon has clearly demonstrated leadership with ArF immersion tools, particularly in the area of 450mm. At SEMICON West this week, a collection of the first fully patterned 450mm wafers – using a Nikon immersion lithography tool — were on display at the newly merged SUNY CNSE/SUNYIT exhibit, booth 517, located in the Moscone Center's South Hall. The Nikon immersion scanner will join existing 450mm infrastructure at the Albany NanoTech Complex in April of 2015 in accordance with the project timeline. This critical milestone will enable G450C founding members and CNSE to perform 10nm and below, full wafer photolithography, while optimizing tool configuration and performance.

The Best of West award-winning NSR-S630D (300mm) ArF Immersion Scanner leverages the well-known Streamlign platform, incorporating further developments in stage, optics, and autofocus technology to deliver unprecedented mix-and-match overlay and focus control with sustained stability to enable the 10/7nm node. The Nikon Corporation booth is in South Hall, Booth 1705.

The NSR-S630D incorporates newly designed optics that deliver multiple levels of active control, while The semiconductor industry is moving to development and high volume manufacturing of sub-10nm generation process devices. Budgets are even tighter at these advanced nodes, making enhanced stability vital. The NSR-S630D leverages established immersion technology, while incorporating key innovations to deliver mix-and-match overlay (MMO) capabilities below 2.5 nm and throughput greater than 250 wafers per hour, in addition to critical overlay and focus with "sustained stability."

The NSR-S630D leverages builds upon the Streamlign platform, incorporating further developments in stage, optics, and autofocus technology to deliver unprecedented performance with "sustained stability" to enable the 10/7nm node. Additionally, the S630D provides world-class throughput ≥ 250 WPH, and is compatible with advanced software solutions that ensure peak manufacturing performance. Significant technical, infrastructure, and business-related issues continue for EUVL, with unclear cost benefits. A 300mm process step and cost comparison for EUVL double patterning (DP) was 2x higher than ArF immersion multiple patterning, and EUV DP results were even less favorable under 450 mm conditions. From the overall cost perspective, new technologies are not always the best approach, and based on 10 years of success, it is believed that 193i immersion will remain the low cost solution moving forward.

The NSR-S630D incorporates newly designed optics that deliver multiple levels of active control, while Multipoint High Speed phase measurement

interferometry enables adjustment of the lens at intervals to reduce aberrations. These enhanced tuning capabilities enable extremely low wavefront rms. Beyond imaging, overlay and focus control are the critical performance factors for the 10/7nm node.

Single nanometer distortion values have been achieved, which is a major factor in improving overlay/mix-and-match capabilities. In addition, the new NSR-S630D reticle stage uses an encoder servo system to increase accuracy while the wafer stage delivers improved temperature control, coupled with structural and water management innovations to enhance stability. The S630D has demonstrated single machine overlay (SMO) Avg.+3σ below 1.4nm across the lot, with across lot S622D/S630D mix-and-match overlay (MMO) below 2.5nm. Further, the S630D autofocus system employs a narrower sensor pitch and improved edge mapping for better focus uniformity, and minimizes sensor fluctuations and process sensitivities. Together these factors optimize yield and increase edge dies per wafer.

Autofocus performance was verified with uniformity data (3σ) below 7nm (including edge shots) and 5.9 nm for full field shots alone. Intrinsic CD uniformity results below 0.69 nm were also demonstrated for 41nm lines on a 90nm pitch.

At the most advanced nodes, tool stability and process robustness become increasingly critical. Additional calibrations help with this, but they must not compromise productivity. Therefore, long-term inherent tool stability and process robustness must be maintained. The S630D has demonstrated five lot SMO data below 1.7nm (Avg. + 3σ) across a ten-day period, and SMO performance (Avg. + 3σ) below 1.4nm across the lot for both hydrophobic and hydrophilic processes. Additionally, a two week focus stability range of only 5.3 nm max/min was achieved.

Nikon provides a number of "Masters" – automated software solutions that ensure the scanner is performing at its best. These include LNS (lens) Master, OPE Master, CDU Master, and OVL (overlay) Master. LNS Master enables reticle-specific thermal compensation on the scanner. OPE Master uses customer designs and scanner adjustments to provide illumination condition matching for aligning performance across a fleet of scanners and ensuring that one OPC solution works on all of them. CDU Master provides optimization capabilities that enable the scanner to correct for other process window detractors. Because overlay matching plays a central role in multiple patterning applications, OVL Master enables automated grid and distortion matching, as well as automated reticle expansion correction to maximize yield. The NSR-S630D works in tandem with the Masters software to deliver optimized scanner exposure parameters that enhance performance on product wafers. In addition to maximized yield and manufacturing flexibility, enhanced productivity is imperative in making these advanced multiple patterning processes cost effective for chipmakers, and the S630D delivers world-class throughput ≥ 250 wafers per hour (WPH).

Controlling warpage in advanced packaging

Dr. Phil Garrou,
Contributing Editor

As we continue to miniaturize, warpage remains the main problem encountered in all areas of advanced packaging. At ECTC, Kotake of Hitachi Chemical addressed "Ultra low CTE core materials for next generation thin CSPs" They describe ultra low CTE (1.8) core materials (E-770G) which are used to reduce warpage in PoP packages. Hitachi simulations show that the CTE of core materials has more impact that the modulus. Best results are obtained when using the new material E-770G for both core and prepreg.

Kim and co-workers at Amkor reported on "Strip grinding Introduction for thin PoP." Typical PoP used in mobile products consists of a logic function In the bottom package and a memory function in the top package. The most difficult barrier to fabricate the thin PoP is warpage control. Amkor TMV (through mold via) PoP structures can be overmolded or exposed die (to allow for heat sinking). When trying to thin the package, there is a limit to the thinness of the overmold and a limit to the silicon die thickness since thinner die result in die chipping or cracking during handling. In the thin mold cap case, it's not easy to control the package warpage. The warpage can be controlled with a thicker substrate, but this increases the package thickness.

The concept of strip grinding is to grind the mold compound and die together. The advantage of strip grinding is to use normal die thickness and mold cap thickness, thus reducing the risk of thin die handling and narrow mold clearance. Mold flash is eliminated through the grinding methodology. By applying a strip grinding process, a very thin die and mold cap can be easily generated.

Double side molded structures are possible, which help make a balanced structure on top and bottom which tends to improve the warpage performance. Bottom side mold is difficult, because the BGA ball is mounted on the bottom area.

For the double-sided mold process flow, chip attach on the top side and BGA ball attach on the bottom side need to be done first followed by double side mold. The bottom molding is ground until the bottom ball is exposed. To remake a BGA, a second ball attach needs to be performed to generate a proper BGA standoff.

Bchir of Qualcomm discussed "improvement of substrate and package warpage by copper plating optimization." While substrate warpage is typically approached through modification of dielectric material properties (such as CTE, Tg, modulus), layer thicknesses (core, prepreg, solder resist and Cu thickness), and Cu areal density per layer there is also an impact from the Cu plating process. Electroplated Cu thin films have porous grain boundaries, wherein grain boundary volume is strongly dependent on electroplating conditions and subsequent thermal processing. During thermal processing, Cu grains grow and merge, eliminating grain boundaries and causing shrinkage. The residual stress in the initial deposit, coupled with shrinkage during subsequent thermal processing, strongly impacts the warpage of the substrate and package. This is compounded by the inherent front-to-back Cu density imbalance which is typical in substrate design.

Choice of electrolytic Cu plating solution has significant impact on the magnitude of package warpage. The influence of Cu plating solution on warpage is related to the resulting grain size distribution and stress state deposited from a given chemistry. Plating additives can be co-deposited as impurities into the Cu layer, and have been shown to strongly impact residual stress and grain coarsening behavior of the Cu deposit.

They found that reducing the plating current density for a given plating solution led to substantial reduction in package warpage. Also, an increase in the plating current density causes a reduction in the deposited grain size, hence a reduction in current density would lead to larger deposited grains and thus larger grains would mean reduced grain boundary volume, less "shrink" in the Cu layer and lower residual stress in the Cu.

The Significance of IBM's EUV Benchmark

Vivek Bakshi, EUV Litho, Inc.

IBM's NXE3300B scanner, at the EUV Center of Excellence in Albany, recently completed a "40W" EUV light source upgrade. The upgrade resulted in better than projected performance with 44W of EUV light being measured at intermediate focus and confirmed in resist at the wafer level. In the first 24 hours of operation after the upgrade, 637 wafer exposures were completed in normal production lot mode with: 20 mJ dose; 83 image fields/wafer (full wafer coverage, including partial die); conventional illumination.

In the process of benchmarking leading edge tools, the performance of the tool is divided into several sections and each part is validated separately. One can divide an EUVL scanner into the major components of optics, source, mask and resist. All parts, except higher power for EUV light source, have been validated for a long time – with challenges remaining but no showstopper. High source power has remained the #1 issue and a potential showstopper. The ~40 W EUV light sources were deployed but have been working at the lower level of 20 W. The validation at 43 W is a ~100% improvement in source power. The previously reported throughput for an EUVL scanner was 200 wafers per day (WPD), so 637 WPD is over three times improvement and exceeds ASML' s own expectation of 500 WPD for 2014.

Dan Corliss, the EUV Development Program Manager for IBM.

The imaging performance of EUV scanners (CD, CDU, pitch, LER) are a function of scanner design, optics, mask, source and resist. The performance of these parts, except source, has been confirmed for some time now and needs no new validation. The source stability has some effect as well on imaging; hence, the power has to be stable and it is one reason for lower power results from the field. However, the #1 issue for EUV has been the throughput of the EUV scanner, which is directly related to the power of the source, as I mentioned above. Although one will eventually test the imaging performance at higher power levels, it does not make sense to be doing that imaging test (and when you know that part works fine) when you are testing for source power upgrade verification – your main challenge. This is how one benchmarks complex machines. As IBM pointed out, it was an unintended but very exciting result of their benchmark, as the focus was to validate higher source power. Other parts of the scanner and the overall imaging performance have been verified by several chip makers for some time.

The next version of the NXE3300B EUV scanner will be potentially used for patterning at the 7 nm and 5 nm nodes. The resolution of printed images will be increased by either multiple patterning (EUV MP), which has been already demonstrated, or via high NA optics (projects are in progress but no demonstration of a high NA EUV tool has occurred yet).

20 mJ of dose for a chemically amplified (CAR) resist, to test the throughput of a EUV scanner, is a very decent dose choice and it is backed by ample data. If this benchmark was done for a 5 mJ CAR resist dose, I will question the test as well, as final images will not meet LER requirements. The good news is that due to recent developments in the high sensitivity resists, now 2-5 mJ dose can give us the same resolution and LER, as from 20 mJ or higher dose CAR resists. In the 2014 SPIE AL meeting, there were many papers confirming the performance of these new types of resists. Hence, the triangle of death (sensitivity, LER and resolution) for CAR resists is no longer valid for these new types of resists. The implications of these new resists are very striking – if we can use these new 5 mJ resists – the throughput will be 3-4 x larger than what is reported for 20 mJ resists. I am hoping that these new high sensitivity resists will mature in another year for HVM use.

Lithography: What are the alternatives to EUV?

PETE SINGER, *Editor-in-Chief*

Hopes remain high for EUV, but long delays has caused attention to shift to various alternatives.

EUV received a recent boost with IBM reporting good results on a 40W light source upgrade to its ASML NXE3300B scanner, at the EUV Center of Excellence in Albany. The upgrade resulted in better than projected performance with 44W of EUV light being measured at intermediate focus and confirmed in resist at the wafer level. In the first 24 hours of operation after the upgrade, 637 wafer exposures were completed in normal production lot mode. Dan Corliss, the EUV Development Program Manager for IBM, called it a "watershed moment."

Critics, most notably analyst Robert Maire of Semiconductor Advisors, said it was "not that much of a real increase in power and certainly no breakthrough, just incremental improvement." He adds: "We still don't have the reticle "ecosystem," the resist and many other components to make for viable, commercial EUV production. We are still a very long way away and this does not change the view that EUV will not be implemented at 10nm." The 10nm node is slated to go into production in late 2015/early 2016.

Yet EUV proponents remain optimistic. Kevin Cummings, the director of lithography at SEMATECH, said "It is good news indeed to hear that IBM in conjunction with ASML has met/exceeded their projected productivity. It is clear to this industry that the EUV LPP source was not meeting the desired schedule and the source improvements timelines were over promised. However this announcement give us some confidence that we are making progress against that schedule. In addition, this milestone is significant in that it allows the wafer throughput needed to continue EUVL HVM development. With the throughputs obtained on the scanner and the recent successes from SEMATECH on zero defect mask blanks and low-dose high-resolution resists now is an excellent time to take advantage of the Albany NY based capability to develop the materials and processes that will be needed for EUVL manufacturing." More analysis of the IBM EUV development can be found in this issue on pg. 13.

Luc Van den hove, president and CEO of imec, described EUV as a cost-effective lithography approach that is "absolutely needed." In terms of imaging performance, imec has been characterizing some of the latest hardware together with ASML and have showed very good resolution performance of 13nm half pitch and 22nm contact holes. "With double patterning, we have even demonstrated 9nm half pitch," Van den hove said. "Who would have thought a couple of years ago that this would be realizable with lithography?"

An Steegen, senior vice president of process technology at imec, said the ideal entry point for EUV is the 10nm node (or N10 using imec's terminology). "If you look at the cost calculation, the best entry point for EUV is actually at N10 because you can replace triple patterning layers in immersion with a single patterning layer in EUV," Steegen said. Since that will come relatively soon with early production occurring toward the end of 2015 and in early 2016, that means that likely the whole development phase will have already been built on immersion and multi-patterning. "Likely you

PETE SINGER *is Editor-in-Chief at Solid State Technology.*

will see on the most difficult levels, a swap, an introduction of EUV at the most critical levels later on in manufacturing for N10," Steegen said.

Interestingly, industry-leader Intel has said that it will not use EUV for 14nm, and even sees a path to 10nm without EUV. At the Intel Developer's Forum in 2012, Mark Bohr, director of Intel's technology and manufacturing group said 10nm "would require quadruple patterning for some mask layers but it's still economical." **FIGURE 1** shows that the use of spacers can enable sub-10nm dimensions without EUV. **FIGURE 2** shows multi-patterning adds to process cost and complexity.

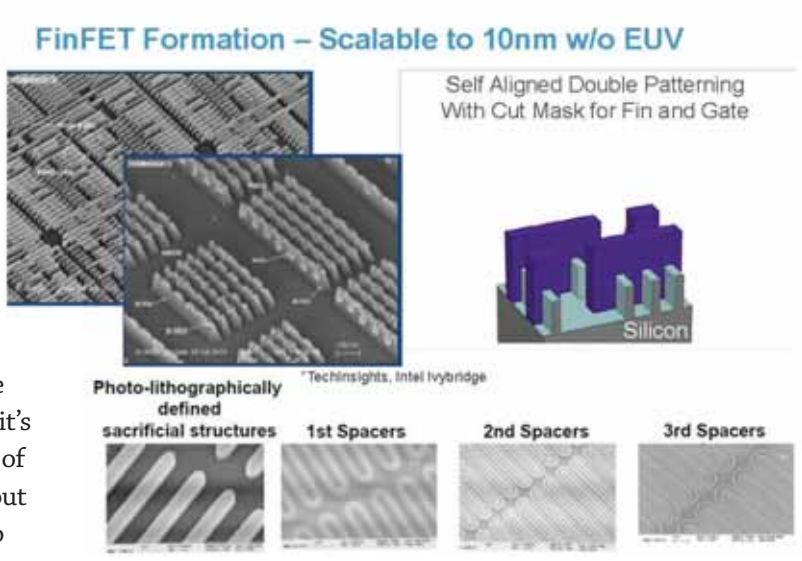

FIGURE 1. Multi-patterning can achieve sub-10nm dimensions. Source: Applied Materials.

Earlier this year, at the SEMI Northeast Forum held in Billerica, MA, Patrick Martin, Senior Technology Director at Applied Materials, talked about scaling and the rising cost and complexity of patterning. "There's a lot of talk in the industry about how scaling is dead," he said. I think a lot of the discussions are if we look at the current architectures entitlements – finFET related technologies that scale to 7nm and 5nm, and the complexity associated with litho, driving those types of cost models, I would have to agree. But the argument is really going to be on architecture entitlement. How the devices are going to adapt to these pattern complexity limited challenges.

Terry Lee, the chief marketing officer for the DSM/CMP business unit at Applied Materials says continued scaling will not be driven as much by lithography, but by 3D. "Scaling used to be enabled by lithography," he said in a presentation at this year's Semicon West. "What we're seeing is the move to enable scaling using both materials and 3D device architectures." 3D devices include FinFETs, 3D NAND DRAMs with buried word lines and bit lines. These devices represent "the drive to further scale on a third dimension versus scaling using lithography on a horizontal plane," Lee said. Appled Materials recently introduced a several new products aimed at the 3D device market, including the Producer XP Precision CVD system shown on this issue's cover.

"We're really in a dilemma when it comes to semi-related production capability," Martin said. The device features are much smaller than the wavelength that we're using. We're into these complex processing related technologies that require double patterning, triple patterning, multiple patterning. The great equalizer here is EUV. If we can ever get to EUV-related manufacturing capability it gets us to a regime where the devices are relatively the same size as the wavelength of light. The problem is that it's been delayed. The challenge is if it doesn't hit 10nm, we're looking at 7nm. If we start looking at the insertion opportunity for EUV at 7nm and 5nm, we're now below wavelength. 13.5 nm is the wavelength of EUV. The complexities associated with double patterning come back into play," Martin added.

The EUV mask challenge

The next major roadblock to progress in the ongoing push to develop EUV lithography for volume production is the availability of defect-free mask blanks. According to Veeco's Tim Pratt, Senior Director, Marketing, the tools in place today are not capable of producing mask blanks with the kind of yield necessary to support a ramp in EUV. "Based on the yield today, the mask blank manufacturing capacity can't produce enough mask blanks to support the ASML scanners that they're planning to ship," Pratt said. "ASML is going to be delivering some light source upgrades in the field and when those start happening, the effective total wafer throughput of EUV scanners in the field is going to multiply and there's just not the supply of usable mask blanks to be able to support those."

The requirement for 2015 is to have zero blank

defects larger than 62nm. SEMATECH in 2012 reported work showing eight defects larger than 50nm. "A lot of progress being made but the elusive zero defects has not yet been hit," Pratt said. Veeco, which is the sole supplier of EUV multilayer deposition tools, has plans to upgrade the existing Odyssey tool and launch a new platform in the 2017/2018 timeframe.

FIGURE 2 shows an EUV mask, which is considerably more complicated than conventional photomasks.

What could derail the EUV ramp, according to Pratt, is a supply of defect-free mask blanks. "EUV is, despite many years and many dollars of investment, not yet in production. The two main gaps are the EUV light sources and the defects on the mask. As they start to make progress, people start to look more seriously at the list of things to worry about for EUV going to production.

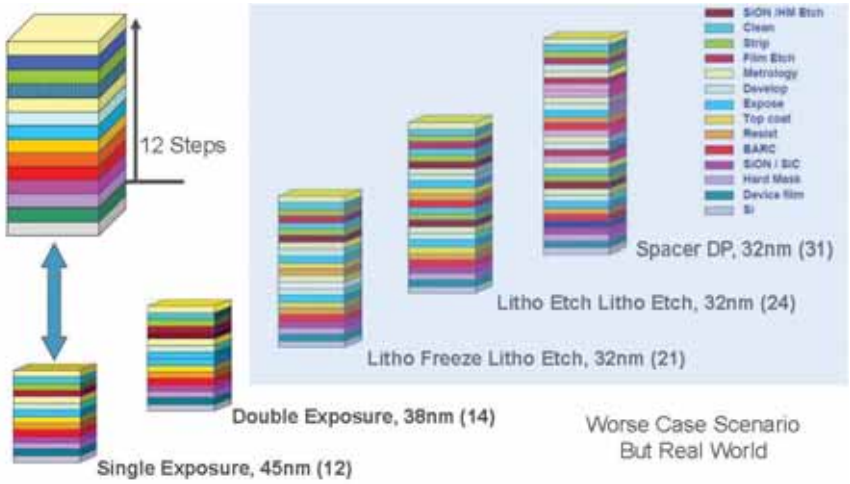

FIGURE 2. Multi-patterning adds many process steps, and cost. Source: ASML.

The e-beam alternative

There are only a few alternatives to EUV and complex (and costly) mutli-patterning approaches: multi-e-beam (MEB), nanoimprint and directed self-assembly.

Electron beam lithography with a single beam has been used for many years for mask writing and device prototyping, and tools available from a number of companies, such as Advantest, IMS, JEOL and Vistec. Single-beam writing has never been able to compete with massively parallel optical systems in throughput and cost. Now, TSMC's Burn Lin says that the time for e-beam lithography has arrived. Why? Digital electronics can affordably provide a gigabit per second data rate in a manageable space, enabling very high wafer throughput. Microelectrical mechanical systems and packaging techniques have advanced sufficiently to support a several order of magnitude increase in beam number and high-speed beam writing. And e-beam techniques generally offer higher resolution than optical systems. [1] Last year, TSMC and KLA-Tencor presented a reflective e-beam lithography (REBL) system that can potentially enable multiple-e-beam direct-write for high-volume manufacturing.

He reported that EBDW could also be used instead of EUV for the complementary solution to break the continuity of the grating made using 193i with pitch division. In addition to again maintaining the benefits of mature 193i on the critical layer, this solution has lower mask costs (no mask required for grating cutting and vias), and the escalating cost of the mask-making infrastructure is avoided.

Multiple beam systems are also being developed by Multibeam Corp. (the well known David Lam is CEO), IMS and MAPPER. MAPPER was founded in 2000 by Professor Pieter Kruit and two of his recent graduates Marco Wieland and Bert Jan Kampherbeek.

What's intriguing about e-beam direct write is that it could be used in conjunction with more conventional immersion lithography. Yan Borodovsky, Intel Corporation Sr. Fellow and Director of Advanced Lithography, calls it "complementary lithography." He says that EBDW could be used instead of EUV to break the continuity of the grating made using 193i with pitch division. In addition to again maintaining the benefits of mature 193i on the critical layer, this solution has lower mask costs (no mask required for grating cutting and vias), and the escalating cost of the mask-making infrastructure is avoided.

An organization that is focused on developing e-beam technology for mask writing and direct write is the E-beam Initiative (www.ebeam.org).

Nanoimprint

Step and Flash Imprint Lithography (SFIL), a form of

ultraviolet nanoimprint lithography (UV-NIL), is recognized for its resolution and patterning abilities. It is one of the few next generation lithography techniques capable of meeting the resolution requirements of future semiconductor devices. Austin-based Molecular Imprints, now a wholly owned subsidiary of Canon, has successfully commercialized the technology. Molecular Imprints invested $165 million over the last decade on platforms, materials, templates and applications.

In 2004, Canon began conducting research into nanoimprint technology to realize sub-20nm high-resolution processes began carrying out joint development with Molecular Imprints and a major semiconductor manufacturer in 2009. Canon says NIL offers such benefits as high-resolution performance, exceptional alignment accuracy and low cost. However, others report that many integration issues such as defectivity, throughput, and overlay must be resolved before SFIL can be used for leading-edge semiconductor high volume manufacturing.

DSA is very promising

Imec's Van den hove described direct self-assembly (DSA) as "very promising" and Steegen said work there has largely focused on reducing defectivity. In DSA, resists that contain block copolymers are deposited on top of guiding structures. The self-directed nature of the process results in very regular patterns with very high resolution.

The trick with DSA is that it requires a double exposure to take away the random patterns at the edge of the device, and the resolution needed for this "cut mask" is also very high. "We're convinced that it's not a replacement for EUV or any high resolution lithography technique. We are very convinced it will be used in conjunction with EUV," Van den hove said. "It certainly keeps the pressure on EUV very high."

Steegen described DSA as a complimentary litho technique that is having quite some momentum. The process starts with a "relaxed" guiding pattern on your wafer. Then, depending on the polymer length in the block copolymer, the space in between the guiding structure is replicated into multiple lines and spaces. "The defectivity of these materials are going to be key to bring the defects down. Our year end target is 60 defects/cm^2 and this needs to go down even further next year," she said.

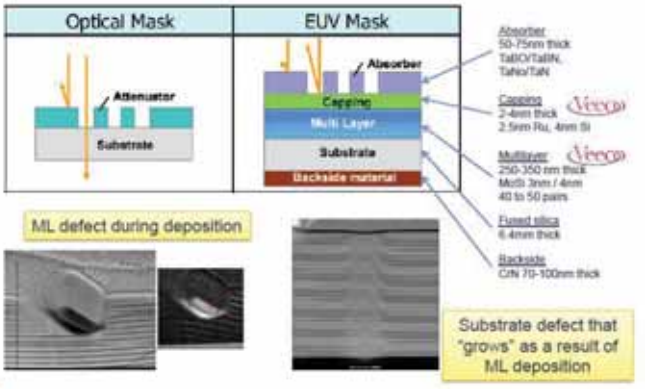

FIGURE 3. EUV masks are considerably more complicated than conventional photomasks. Source: Veeco.

Work at imec has shown that the polymers, with a hard mask on top, are robust enough to enable the etching of the patterns into silicon. "That's fairly new data and very promising," Steegen said. Imec is already looking at where DSA levels could be inserted into the logic N7 flow, with fins and spacers being primary targets. Steegen said the Metal1 level would be a challenge due to its irregular pattern. "That makes it not easy to be replaced with DSA, but we're looking into techniques to do that," she said.

Here's how imec summed up DSA readiness:

- Good progress in material selection and integration flow optimization for line-multiplication down to 14nm, pattern transfer into bulk Si demonstrated.
- First templated DSA process available using SOG/SOC hard mask stack.
- Focus on defectivity reduction & understanding, currently at 350 defects/cm^2, YE13 target 60 def/cm^2

Conclusion

Hopes remain high for EUV, but long delays has caused attention to shift to possible alternatives. Multi-level patterning is costly but it works. Meanwhile, results from early work into directed self-assembly (DSA) is quite promising. DSA could be used in conjunction with EUV for the 7nm node, scheduled to go into production in the 2017/2018 timeframe. Some new device structures, such as vertical NAND and FinFETs, take the pressure off of lithography, but create challenges in other process areas, such as deposition and etch.

Gas applications in lithography

KLAUS HEGE, *Linde Electronics, Munich, Germany*

While gas mixtures for laser sources are the most obvious gas-related processes in lithography, there are also applications for nitrogen, helium, carbon dioxide and hydrogen.

Lithography is a key enabling process with very demanding requirements. Shrinking feature sizes will raise the bar even further. These increasing requirements on the process side will lead to increasing quality requirements for materials. This article provides an overview of existing gas applications in lithography and implications for the future.

Photolithography is a key enabling and very critical process during semiconductor chip manufacturing. It always occurs at the beginning, and any defect occurring during the lithography process impacts the quality of subsequent process steps.

Smaller feature sizes require a better optical resolution. As the resolution depends on the wavelength of the light, illuminating systems with increasingly smaller wavelengths had to be developed. The current lowest available wavelengths for high-volume manufacturing are193nm and 248nm and are used at the most critical layers.

Excimer lasers

The light sources used to produce the desired wavelengths are excimer gas lasers and are fed with gas mixtures containing halogens and noble gases. Krypton-Fluorine excimer lasers emit light with 248nm, while Argon-Fluorine lasers generate photons at 193nm. Both belong to the Deep Ultraviolet part of the spectrum and are therefore called DUV lasers (in contrast to EUV, which is Extreme Ultraviolet light).

High-precision starting materials

As the requirements on the precision of the lithography process are getting higher, equally precise quality control of the laser gas source material is mandatory.

Meeting the stringent requirements for mixture accuracy and gas purity are crucial for a high-quality light generation process. Gas contaminations as well as non-precise gas mixtures affect critical laser parameter like power output, target wavelengths, and lifetime.

Other gas applications within lithography

While gas mixtures for laser sources are probably the most obvious gas-related processes in lithography, there are a couple of well-established and a few rather new gas applications:

- Nitrogen for general purging
- Helium for heat transfer (cooling)
- Carbon dioxide as a laser gas and for latest-generation, defect-free illumination
- Hydrogen as a cleaning and shielding gas for EUV lithography

Nitrogen for general purging

Nitrogen is the most commonly used inert gas. The purity requirements of the lithography application are very demanding, requiring multiple-step purification.

Nitrogen is supplied to semiconductor fabs by

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on-site generation or in cluster parks by pipeline. On-site plants use cryogenic distillation to take nitrogen from the air, which contains 78%, and purify it to 99.999%. Gas companies have standard plants available for up to 50,000 m3/h capacity. Some plant designs enable purity of 99.9999%, which saves equipment and power costs for additional purifiers.

Helium for cooling

Helium is used for cooling optical lenses in lithography. As the helium content in air is very small (0.0005%), it is not economical to extract it from the air. Instead, Helium is extracted from natural gas sources. Having access to several sources spread out globally can enable a secure supply.

As Helium is a limited resource, some industrial gas companies have developed solutions for Helium recovery, which makes possible the re-use of this scarce material.

Carbon dioxide for immersion and EUV lithography

Carbon dioxide has had many applications in the industrial gas industry, but its use in lithography is fairly recent.

In state-of-the-art immersion tools, CO2 substitutes some CDA (clean dry air) to prevent the "big bubble effect." CDA has been used to shield the immersion hood against ambient air, but can form bubbles in the waters, which can potentially deflect the light beam and then cause defects in return. This effect gets more pronounced for smaller nodes for two reasons:

- Smaller features are more affected by even small deviations of the light beam.
- The increasing use of multi-patterning leads to higher throughput requirements, which then leads to a faster scan speed with the increasing risk of entrapping more CDA bubbles.

CO2, with its superior chemical/physical properties (compared to CDA), does not form big bubbles. As CO2 is applied at a critical spot (at the wafer/photoresist/lens interface), there are very stringent gas quality requirements.

For EUV, CO2 is used as a laser gas. The new source architecture is changing the light generation concept, switching from a direct light source (excimer lasers) to an indirect light generation (a CO2 laser beam hitting a tin droplet, leading to the generation of EUV light).

While these two applications require the same molecule (CO2), the application and purity requirements are totally different. Having several different types of sources (ranging from natural wells over industrial production to biochemical routes) is challenging, as all these sources have unique types of contaminations. Gas companies can supply CO2 as ultra-high purity gas (99.9997%) or as food grade, which is then purified on-site.

As the CO2 production and purification is mostly designed to meet the requirements of the beverage and food industry, this does not automatically guarantee that a specific source is equally suited for semiconductor applications.

A tight quality control is therefore crucial, not only verifying food criteria, but also meeting the needs of the semiconductor industry. As an alternative to food quality, higher grades are available like 6N (= 99.9999%) and better.

Hydrogen as a cleaning and shielding gas

The development of EUV as a next generation lithography technology is proceeding. The small wavelength of 13.5nm will enable customers to process wafers for 10nm, 7nm, and smaller nodes.

EUV uses a different light source architecture, involving liquid tin droplets. These tin droplets can cause tin depositions on the reflecting optics, leading to a reduction in light power. To prevent this, Hydrogen is used to form volatile tin compounds, which can be pumped away, preventing a reduction in the amount of photons available for illumination. Compared to other gases like Nitrogen, Hydrogen has a low absorbance for EUV light, making it the gas of choice wherever a EUV light beam is passing through a chamber.

10nm success depends on concurrent design and development

TOM QUAN, *Deputy Director, TSMC*

New approaches to start-ups can unlock mega-trend opportunities.

The Prophets of Doom greet every new process node with a chorus of dire warnings about the end of scaling, catastrophic thermal effects, parasitics run amok and . . . you know the rest. The fact that they have been wrong for decades has not diminished their enthusiasm for criticism, and we should expect to hear from them again with the move to 10nm design.

Like any advanced technology transition, 10nm will be challenging, but we need it to happen. Design and process innovation march hand in hand to fuel the remarkable progress of the worldwide electronics industry, clearly demonstrated by the evolution of mobile phones since their introduction (**FIGURE 1**).

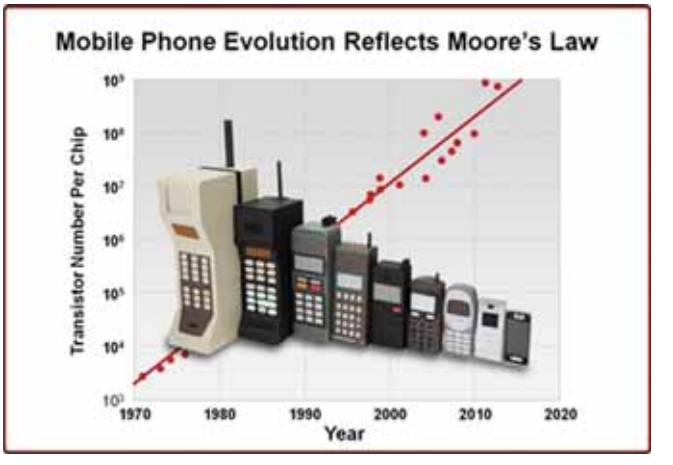

FIGURE 1. The evolution of mobile phones since their introduction.

Each generation gets harder. There are two different sets of challenges included with a new process node: the process technology issues and the ecosystem issues.

Process technology challenges include:

- Lithography: continue to scale 193nm immersion
- Device: continue to deliver 25-30% speed gain at the same or reduced power
- Interconnect: address escalating parasitics
- Production: ramp volume in time to meet end-customer demand
- Integration of multiple technologies for future systems

Ecosystem challenges include:

- Quality: optimize design trade-off to best utilize technology
- Complexity: tackle rising technology and design complexity
- Schedule: shortened development runway to meet product market window

Adding to these challenges at 10nm is that things get a whole lot more expensive, threatening to upset the traditional benefits of Moore's Law. We can overcome the technical hurdles but at what cost? At 10nm and below from a process point of view, we can provide PPA improvements but development costs will be high so we need to find the best solutions. Every penny will count at 7nm and 10nm.

TOM QUAN *is Deputy Director, TSMC, San Jose, CA.*

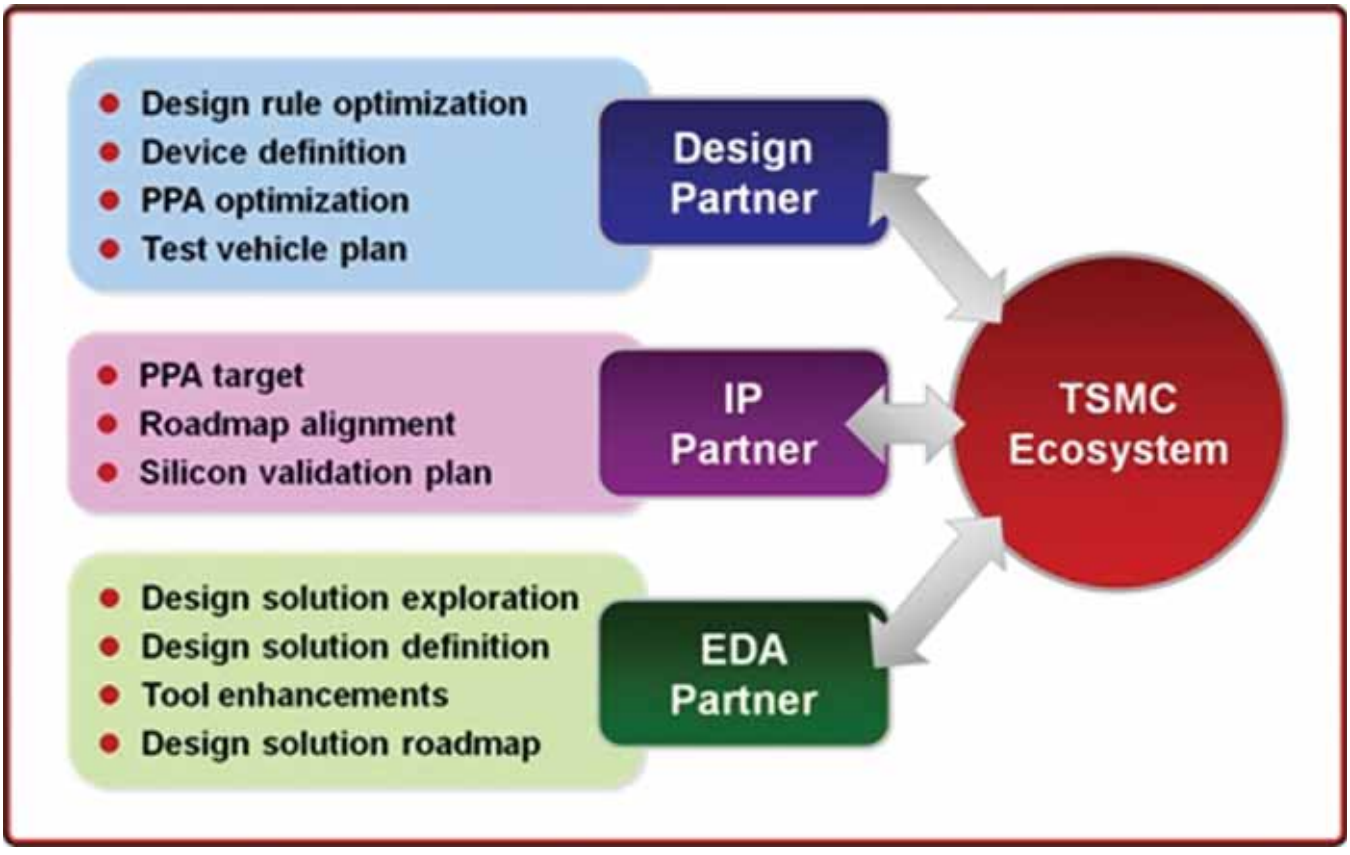

FIGURE 2. A new design ecosystem collaboration model is needed due to increasing complexity and shrinking development runways.

Design used to be fairly straightforward for a given technology. The best local optimum was also the best overall optimum: shortest wire length is best; best gate-density equates to the best area scaling; designing on best technology results in the best cost.

But these rules no longer apply. For example, sub-10nm issues test conventional wisdom since globalized effects can no longer be resolved by localized approaches. Everything has to be co-optimized; to keep PPA scaling at 10nm and beyond requires tighter integration between process, design, EDA and IP. Increasing complexity and shrinking development runways call for a new design ecosystem collaboration model (**FIGURE 2**).

Our research and pathfinding teams have been working on disruptive new transistor architectures and materials beyond HKMG and FinFET to enable further energy efficient CMOS scaling. In the future, gate-all-around or narrowwire transistor could be the ultimate device structure. High mobility Ge and III-V channel materials are promising for 0.5V and below operations.

Scaling in the sub-10nm era is more challenging and costly than ever, presenting real opportunities for out-of-box thinking and approaches within the design ecosystem. There is also great promise in wafer-level integration of multiple technologies, paving the way for future systems beyond SoC.

A strong, comprehensive and collaborative ecosystem is the best way to unleash our collective power to turn the designer's vision into reality.

Rigorously tuned compact models: Extending predictive models to full-chip

WOLFGANG DEMMERLE, THOMAS SCHMÖLLER, HUA SONG *and* **JIM SHIELY,** *Synopsys, Aschheim, Germany, Mountain View, CA and Hillsboro, OR.*

Fast and predictive 3D resist compact models are needed for OPC applications. A methodology to build such models is described, starting from a 3D bulk image, and including resist interface effects such as diffusion.

With further shrinking dimensions in advanced semiconductor integrated device manufacturing, 3D effects become increasingly important. Transistor architecture is being extended into the third dimension, such as in FinFETs [1], multi-patterning techniques are adding complexity to lithographic imaging in combination with substrate topography.

Even on planar wafer stacks, process control gets more and more challenging for the 1X nm technology node, as features are being scaled down while exposure conditions remain at 193nm immersion lithography with 1.35 NA. Image contrast decreases, especially at defocus, resulting in high susceptibility for resist loss height and tapered sidewalls; resist profiles may deviate significantly from ideality. Although imaging conditions can be well controlled at nominal exposure conditions, the effect on the process window is usually substantial, as the useful depth of focus as become comparable to the resist film thickness. These dependencies are illustrated in **FIGURE 1**.

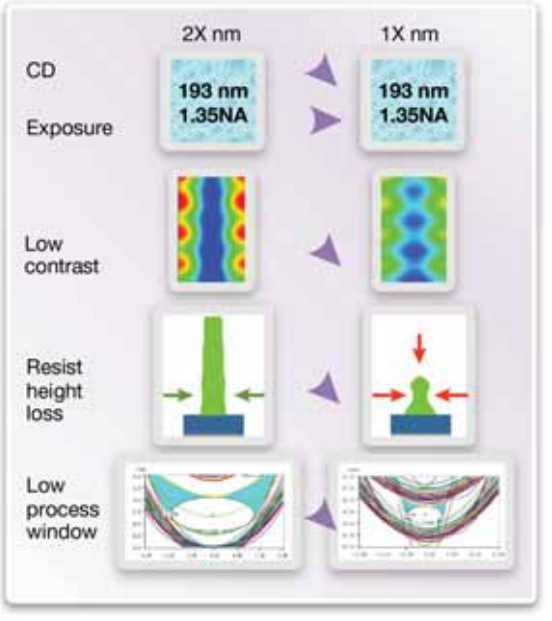

FIGURE 1. Extending 193nm immersion technology to the 1x technology node reveals new patterning challenges.

Especially random 2D layout structures exhibit weak image areas, where often severe resist top loss or footing occurs, which can results in critical defects within the subsequent etch process. An example for such a weak spot is shown in **FIGURE 2a**, taken during the early phase of process development [2]. The left clip shows a top-down SEM image of the pattern in resist, taken

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after the development step. It does not provide any indication for a potential defect in this area. Conventional 2D models represent well the bottom contour of the resist profile. Overlaying the model contour (red line) with the SEM image shows a very good correlation with reality, again giving no motive to apply any layout corrections. However, after etch a bridging hot spot is revealed, as can be seen on right SEM image. A more detailed analysis of the weak spot area using rigorous simulations indicates a low image contrast and severe resist loss of about 60% at the critical location, as shown in **FIGURE 2b**. Degenerated 3D resist profiles

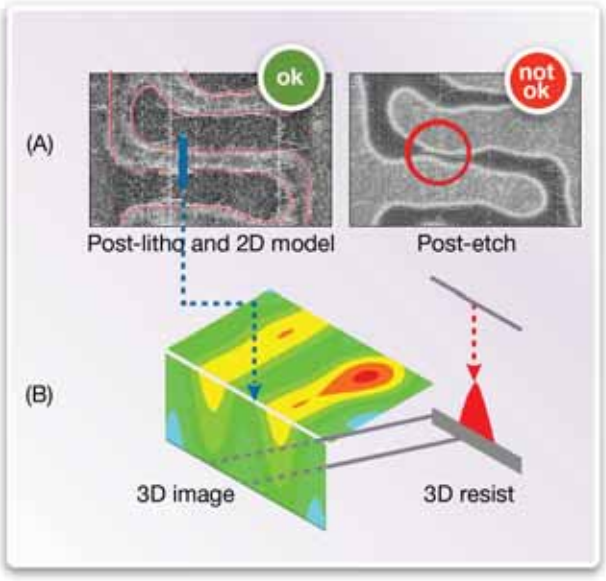

FIGURE 2. "Weak lithography spot" often becomes only visible after etch if 2D models are used for correction and verification.

are one of the main root causes for post-etch hotspots at advanced technology nodes.

In case those "weak litho spots" in a layout are known, localized corrections to mask features can be applied to prevent yield loss. However, the diversity of random logic structures in advanced designs makes is mandatory that compact models are available which reflect the 3D nature of the resist profiles at any location within the chip, and that this information is being utilized during optical proximity correction and verification, on full chip scale. Rigorously tuned compact models provide an efficient approach to achieve this goal, as we are going outline in the subsequent sections.

Efficient generation of 3D resist compact models

The fundamentals of 3D resist simulation are well captured by rigorous lithography process simulation which is based on a first principle physical modeling approach [3 - 6]. The corresponding simulation results do not only provide an accurate representation of the expected 3D resist profile for arbitrary device patterns within a random layout context. Rigorous models are also capable of predicting the impact of process variations such as focus or dose shifts, wafer stack or illumination condition changes, to only name a few, onto the lithographic performance. This predictive power is achieved by properly separating the various contributions to pattern formation inside the models, for instance addressing optical effects and resist effects individually. Due to their physical nature, the accuracy of optical simulations is only limited by the quality of the input data charactering the optical conditions in the exposure tool. As chemical processes in the photo resist are rather complex, the corresponding models utilize a small set of free, physically or chemically motivated parameters. Only a few experimental data points, e.g. from SEM metrology, are required to calibrate those free parameters, ensuring a good match between experiment and simulation over a wide application space. However, this predictive simulation power comes at the expense of run time – the enormous demand for computational resources does not allow rigorous models at to be applied on a full chip scale.

Standard full chip mask synthesis applications such as optical proximity correction (OPC) or verification are based on the deployment of conventional 2D compact models, i.e. models which represent the resist contours visible in a top-down views. Compact models are optimized for performance. Their accuracy, i.e. the match between model and experiment, is usually achieved by optimizing a large set of fitting parameters, inputting an even larger metrology data set based on CD-SEM measurements. Expansions to a models application space, e.g. to cover additional feature types, are enabled by extending the training data set for model fitting. However, this approach has limitations, as the effort for gathering additional metrology data might become prohibitive, which is rather cogent in the case of 3D metrology.

However, as outlined above, 3D models are required

to capture hotspots which are being introduced through local resist height loss. An obvious extension into the third, vertical dimension could be to build individual 2D models at different image depths, representing resist contours of a 3D profile at discrete resist heights. The application of any of the individual 2D models to downstream OPC/LRC tools is straightforward. However, the relevant image depths need be determined in advance due to the discrete nature of the methodology itself. The critical resist heights can be predetermined, based on etch process results. In practice, a bottom model along with one or two models at critical heights are usually sufficient to detect sites where etch results become sensitive to resist profile. Then the models are directly calibrated on those critical resist heights [7].

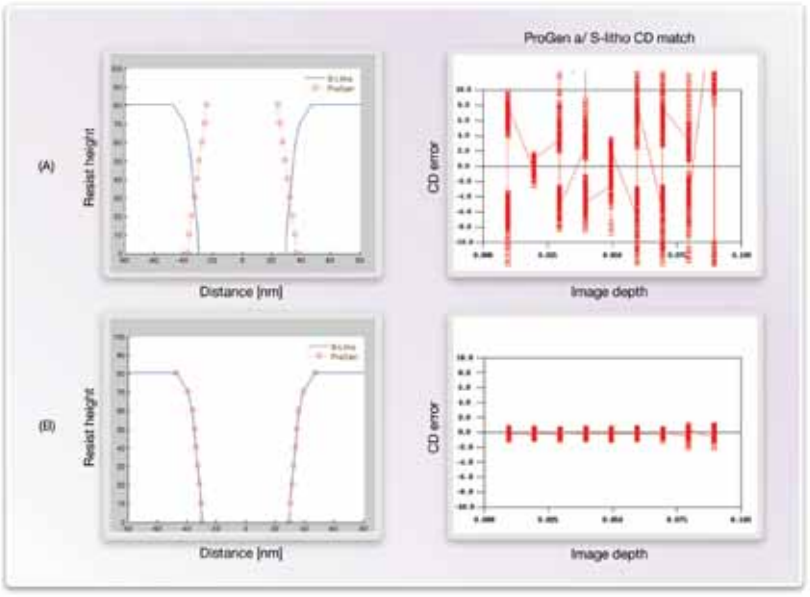

FIGURE 3. Matching 3D resist compact model profiles to rigorous reference data.

One major challenge to support this compact model calibration approach is the preparation of the corresponding metrology data. Conventional, single plane 2D models already require a significant amount of top-down CD-SEM data based on a feature set large enough to represent the entire design space. However, only very rough estimations can be made about the actual resist profiles. This is not sufficient for a reliable 3D model calibration.

Several techniques are available to experimentally characterize the three-dimensional shape of a resist profile, such as atomic force microscope (AFM) or CD-SEM cross section measurements. Common to all these methods is that they are very complex, elaborate, and costly, and therefore not suitable for high volume metrology data collection.

Alternatively, a carefully calibrated rigorous simulator model can be used to generate virtual 3D resist profile data by outputting CD values at specific heights, for specific features. Due to the underlying physical modeling approach, only significantly less experimental data are required for resist model calibration, compared to compact model building [8]. A typical calibration data set consists of CD-SEM top down measurements on a small set of 1D structures, covering critical CDs and pitches, through process window. In addition, a few 3D reference data points, e.g. from AFM, cross section measurements, or etch fingerprints are used to tune the absolute resist height of the profiles in order to match experiment and simulations in all dimensions. This approach not only removes the potential risk of measurement inconsistency between 2D and 3D metrology results, but also opens the door for extensive data collecting with minimum fab efforts.

The CD data sets, either experimentally determined virtually generated for a number of discrete heights, is then fed to compact model calibration at multiple imaging planes. The calibration can be independent for each height. It is often found that fitting a separate threshold for each resist height enables a better match between input data and compact model results. This is mainly due to the fact that vertical resist physics, such as z-diffusion, out-diffusion at boundaries are not included in the traditional compact modeling approach. Differences are compensated through a variable threshold. In addition, other resist models parameters may also be varied to compensate the z-direction physical effects. As a result, the common physicality of the model is compromised, as over-fitting takes place.

In order to demonstrate these dependencies, rigorous simulations based on a calibrated resist model were used to generate reference CD data for over 500 gauges at 9 height positions in the resist film. The

gauges represent real fab process covering both 1 dimensional and 2 dimensional layout patterns. The process settings between compact model (ProGen) and rigorous model (S-Litho) are matched exactly. **FIGURE 3a** shows the results of a compact model calibration in which threshold and common resist model parameters were kept constant for all sampling heights. The example profile (left image) shows a clear mismatch between the two modeling approaches, which results in an overall matching error with a root-mean-square (RMS) value of 2.9nm for the entire data set (right image).

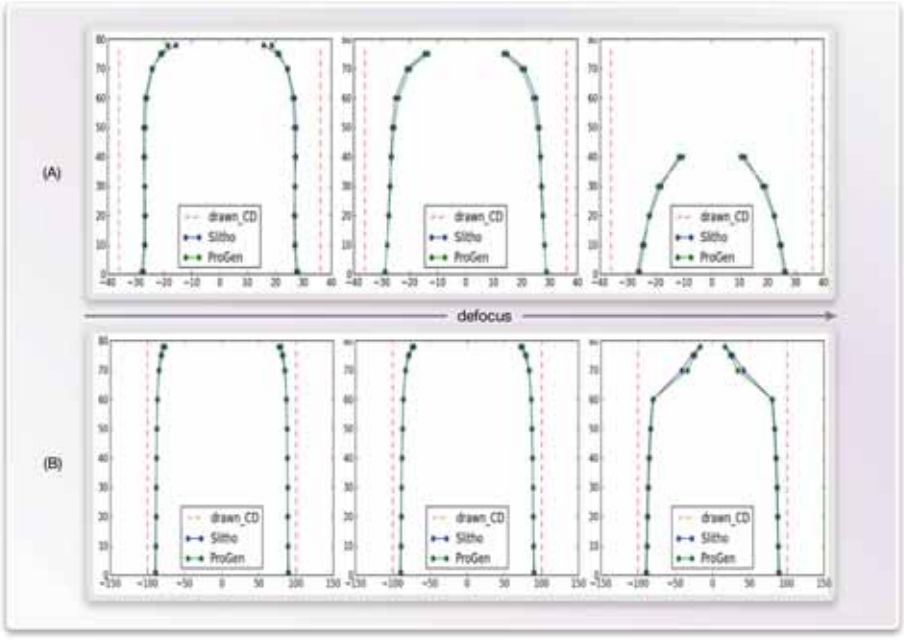

FIGURE 4. Rigorously tuned 3D resist compact models can predict the impact of process variation on profiles without additional data fitting.

These limitations have been overcome by adopting more physical modeling approaches, as used in rigorous simulators, while keeping the model form compact for full-chip applications. To that end, the bulk image is calculated by using one set of retained Hopkins kernels. Optical intensity can be assessed at any image depth without accuracy compromise. Based on an accurate bulk image, the model has been extended to capture effects present in chemically amplified resists. For instance, acid generation, acid-base neutralization, and lateral as well as vertical diffusion are taking into account. Specific boundary conditions at the resist interfaces are used to account for surface effects. The model is formulated in a continuous form so that a model slice at any image depth is readily available for use after calibration. While the calibration data is collected at discrete image planes, all planes are calibrated simultaneously using one set of resist parameters to guarantee physical commonality among them. Moreover, the calibration is done stepwise carefully to ensure the optical part to account for optical effects and resist model to account for resist effects.

The corresponding results are shown in **FIGURE 3b**. The compact modeling approach now takes vertical diffusion effects into account, including out-diffusion at resist top and bottom, which ensures an excellent match for individual profiles (left image) as well as for the entire data set, resulting in an rms value of 0.5nm.

Compact resist model portability

The integration of physical effects into compact modeling does not only enable the extension of resist simulation into the third, i.e. the vertical dimension, as described in the previous section. Characteristics such as "portability" or "separability", usually assigned to rigorous models only, become now available within compact modeling as well. Rather than lumping optical and resist effects into a single set of model fitting parameters, the optical set is characterized individually, and resist effects are modeled individually, and therefore separated from the optical contributions to the modeling result. The more clean the separation, the more accurate is the modeling of the resist system response to slight modified optical condition, i.e. conditions different from the ones present during calibration.

Typical simple changes to the optical setup are the variation of focus and exposure dose. **FIGURE 4** shows the 3D profile results for two representative features of lines & spaces (L&S) data set, a narrow line with a nominal CD of 60 nm (Figure 4(a)) and a wide line with a nominal CD of 200 nm (Figure 4(b)). The calibration was done on 56 L&S pattern, at nominal focus (Figure

4, center images), with profiles being sampled at various heights. In order to test compact model prediction, we have applied a negative focus offset (Figure 4, left images), and a positive focus offset (right images), and compared the compact model results to profiles determined by rigorous simulation, which served as a reference. The profile changes through focus are very well captured by the compact model, especially the resist top loss at positive defocus (Figure 4, right images). These results are already a first demonstration of predictive power which comes with rigorously tuned compact models. In similar experiments, we have also successfully shown that this modeling concept can be utilized to investigate unintended printing of sub-resolution assist features by analyzing the 3D resist response [9], and to source variations [10].

3D resist model based proximity correction

An accurate and predictive 3D resist compact model can be deployed in mask synthesis verification, or lithographic rule check (LRC), to detect weaknesses in resist profiles. For severe hot spots, simple OPC retargeting is not sufficient to mitigate issues caused by degraded resist profiles. In such a case, the application of rigorously tuned 3D compact models within optical proximity correction (OPC) offers an efficient approach to automatically repair hotspots within the mask synthesis flow. ProGen models exhibit the unique property of being consistently applicable in combination with different mask correction approaches, for instance conventional OPC as well as inverse lithography technology (ILT).

FIGURE 5a shows such a weak spot on an ILT mask where the correction is based on a 2D resist compact model, just the contours representing the bottom of the resist profile (black contour). However, the 3D rigorous simulation results reveals severe resist pinching at the top of the resist bulk, as displayed in Figures 5b. Looking at the bottom contour alone, such a hotspot would not have been detected. The red contour in Figure 5a represents the corresponding 3D compact model result extracted at the resist top, confirming the rigorous simulation result. Consequently, in order to achieve a more robust mask solution, we are now taking information from the entire resist profile into the ILT cost function to compute the corresponding correction.

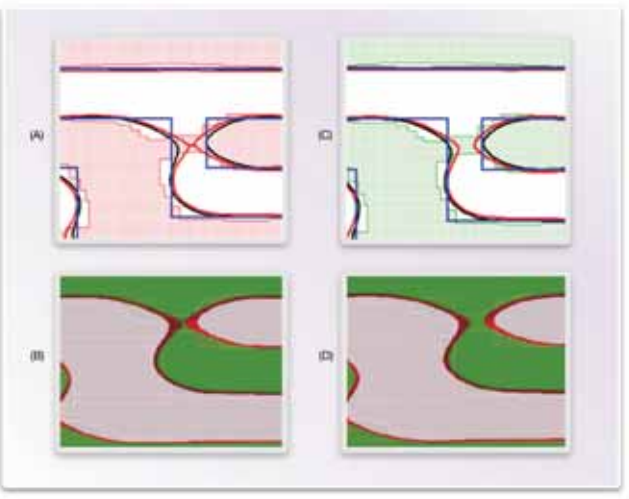

FIGURE 5. Successful OPC correction of an ILT mask, based on 3D resist compact model input.

The results are shown in Figure 5(c), including bottom resist contour (black) and top resist contour (red) for the modified mask. Although the resist profile sidewall that the location of the weak spot still show some taping, the situation has significant improved over the 2D model based correction. This is confirmed by the rigorous simulation results in Figure 5(d), which does not show indications for resist pinching anymore.

The above OPC results conducted by ILT using 3D resist models again imply that resist profile weakness can be corrected in a mask synthesis process with the help of one predictive, accurate 3D resist compact model. As a result, wafer yields will be greatly improved.

Summary and outlook

In this work, we have outlined the concept of using a rigorous simulation approach to tune and improve compact modeling capabilities. Characteristics such as "predictivity", "portability" or "separability", usually known only within the context of physical models, can be transferred to compact models and therefore made available for full chip mask synthesis applications. We have successfully demonstrated this approach by establishing rigorously tuned 3D resist compact models. Those models combine the performance benefit of compact models, required for full chip mask synthesis applications, with the 3D modeling capabilities and predictivity of rigorous models. We have demonstrated that the rigorously tuned resist model can be carried to a different lithography process setup, e.g. a

different illumination source without suffering any accuracy degradation. Those models can be deployed in downstream mask synthesis applications such as optical proximity correction or verification without further modifications. As an example, we have performed a 3D resist model assisted mask correction, using ILT, to mitigate potential post etch hotspots.

The concept of "rigorously tuned compact models" can be easily extended to address other simulation challenges, even beyond the litho process, as shown in **FIGURE 6**. In fact, it has already been used to improve mask topography simulation capabilities in compact models, or extend resist modeling properties to capture effects which are characteristic to negative tone development. We are currently working on utilizing TCAD physical etch simulation to tune etch compact models, which will take simulated 3D resist profiles as input. A combination of TCAD etch tools and rigorous litho simulation can be used to generate compact models which take underlying wafer topography into account.

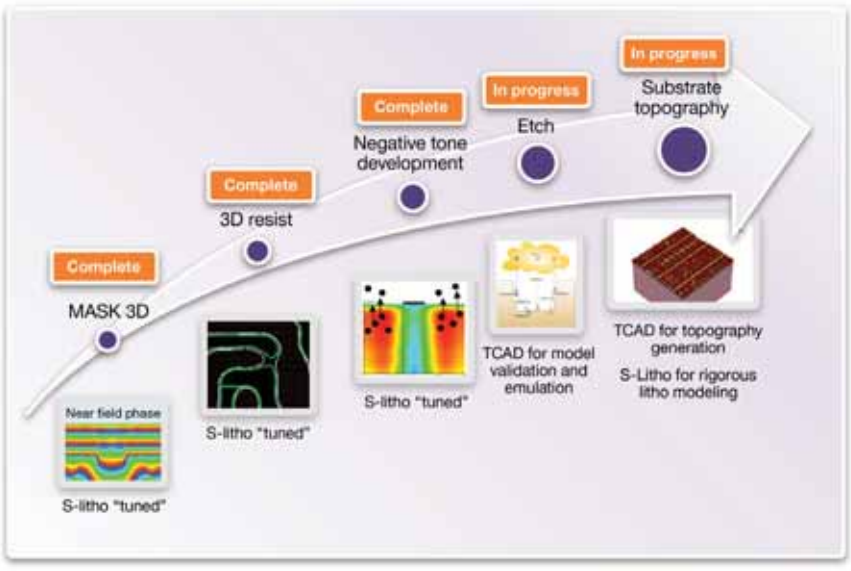

FIGURE 6. Extending the concept of "rigorous tuning" to process simulation beyond traditional lithography.

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Global shutter image sensors

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Different GS pixel architectures and technologies are presented and performances compared.

CMOS image sensors are in widespread use today in many consumer and professional applications. The typical shutter type for most CMOS image sensors is a so-called Rolling Shutter (RS). This is an inherent property of the 4T active pixel and its derived architectures with shared amplifier readout. The main drawback of a RS CMOS imager is that the start and the stop of the exposure is slightly shifted from pixel line to pixel line resulting in object deformation of fast moving objects (**FIGURE 1**) or the so-called "jello" effect when the camera is vibrating. To avoid this, either a mechanical shutter or a flash is required. Neither of these is accepted in many applications.

The alternative is using a so-called Global Shutter (GS) pixel based image sensor, whereby every pixel of the entire pixel array acquires the image during the same time period. This requires an in-pixel memory element that stores the signal after capture by the photodiode. Interline transfer (IT) CCDs were for many years the technology of choice for GS imagers, due to the combination of global shutter with low read noise through a correlated double sampling (CDS) output stage. However, compared to CMOS image sensors, CCDs are limited to moderate readout speeds, consume more power, and lack on-chip integration of timing and AD conversion circuitry.

The first generation of GS CMOS imagers suffered from high read noise due to the lack of CDS on the charge sense node, and from poor shutter efficiency. Today, several techniques have been proposed to combine CDS with GS functionality. Meanwhile, pixel scaling efforts and microlens designs allow recovering the loss in fill factor caused by the in-pixel storage elements required in GS pixels, and allowed low-noise GS pixel design with good shutter efficiency. Shutter efficiency reports how much the stored pixel value is distorted by incoming light (which will be typically light from an unrelated exposure period which falls on the pixel when awaiting readout). It is calculated as {1 – sensitivity with shutter closed / sensitivity with shutter open} and can typically be wavelength dependent.

FIGURE 1. Rolling shutter image artifacts in the spokes of the turning wheel

FIGURE 2 shows two global shutter pixels of earlier generations. Fig. 2a is a 5-transistor global shutter pixel, which stores the image on floating diffusion FD after exposure. At readout, the value sampled on FD is read through the source follower when the pixel row is selected. Then the floating diffusion is reset, and a reference level is read from the pixel. This reference level cancels any random fixed offset variations between pixels, which would otherwise cause fixed pattern noise. However, the temporal kTC noise on the floating diffusion sense node is not cancelled, since the reference for each pixel is taken after reading the photosignal, by a new reset of the sense node, which introduces a new random offset error

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uncorrelated to the signal level. Gate TX2 acts as an anti-blooming drain and is also used to start the exposure. The anti-blooming function is important, since excess charges are not allowed to flow to FD, where the pixel data of the previous exposure is stored.

The shutter efficiency of such pixels is not very good, typically below 99.9% for green light. The reasons

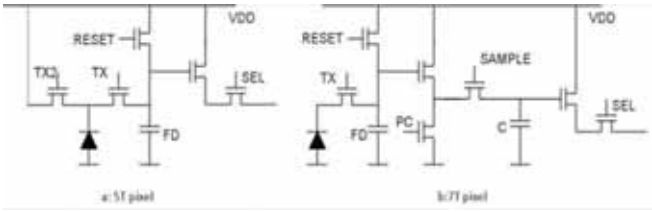

FIGURE 2. 5-transistor charge domain global shutter pixel (a) and 7-transistor charge domain global shutter pixel (b).

why are shown in fig. 3, which is a cross-section of the 5T pixel structure. Photons generate electrons in the substrate, which diffuse through the substrate until they reach the pinned photodiode as shown in green. Some electrons generated deeper in the substrate may be collected directly by an unrelated n+ junction, such as the n+ junctions of the charge drain or the drain of the reset transistor, as shown in orange. These charges do not contribute to the photosignal and result in a loss of quantum efficiency. Some charges may diffuse to the junction of the floating diffusion, rather than by the photodiode, as shown in red. These disturb the signal stored on the floating diffusion and reduce the shutter efficiency.

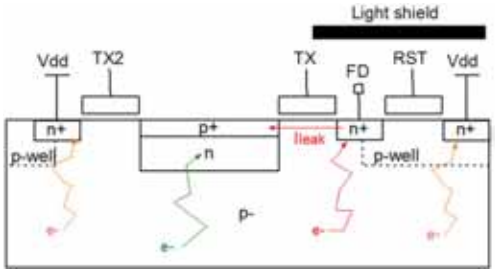

FIGURE 3. cross-section of a 5T charge domain global shutter pixel

This diffusion also explains the wavelength dependency of shutter efficiency for this pixel type: blue light is generated close to the surface, the majority of it inside the pinned photodiode. Part of the electrons generated by red or near infrared light are located deeper in the silicon, and have to diffuse first to the photodiode, but may reach the floating diffusion instead, which results in lower shutter efficiency for these longer wavelengths.

Often, a light shield is placed on top of the storage node to improve shutter efficiency and microlenses are used to focus the light onto the photodiode, away from the storage area. Also, a higher doped p-well under the unrelated n+ junctions can be used to reduce the charge diffusion of electrons, thanks to a small potential difference between the epitaxial p- substrate and this higher doped p-well region. A majority of the electrons will prefer to diffuse to the photodiode, where this barrier is not present.

However, a further effect that reduces shutter efficiency and which is not solved by light shields and neither by this p-well, is that some charge may leak from the photodiode through the transfer gate to the floating diffusion during the next exposure time (see Ileak in **FIGURE 3**). To include this effect in shutter efficiency measurements, it should be measured with constant light in a mode where the pixel integrates the next exposure during readout. Often, shutter efficiency is measured while the photodiode is drained through TX2, which cancels this transfer gate leakage, but which does not match the typical use cases for global shutter pixels in the real world, where a next image is captured during readout of the image. Furthermore, dark leakage current of the floating diffusion junction will also disturb the signal sampled on it and is a further source of noise, hot pixels and non-uniformity. This is especially important since the floating diffusion n+/p junction reaches the surface, where leakage currents will increase due to surface defects present inside the depletion region of the n+/p junction.

Fig. 2b solves the shutter efficiency and dark leakage issues of the storage node by storing the signal in voltage domain on capacitor C behind a first source follower, instead of on the floating diffusion. This capacitor can be larger and be composed of a gate or plate capacitance, which is not capable to collect electrons straight from the substrate, where they are generated by photons. In this way, the shutter efficiency can be improved above 99.98%. The pixel can be operated with double sampling by reading the reset level as a reference after reading the value sampled on C, but it still lacks correlated double sampling, just like the 5T pixel of fig. 2a. And some electrons can be collected from the substrate by the junctions of the switch connecting to the capacitor, which explains why shutter

efficiency is not perfect.

For both pixel types of Fig. 2, the full well charge is proportional to the sense node capacitance, and the noise is proportional to the square root of the sense node capacitance. A typical floating diffusion of 1.6 fF, corresponding with a conversion gain of 100 µV/e-, will operate with a voltage swing of 1V. This corresponds with a saturation level of 10,000 e-. The kTC noise on 1.6 fF is 16 e- RMS. This noise appears both on the signal and reference samples, so it is increased by the square root of 2 (sqrt(2)) to 23 e- RMS at the sensor output. The dynamic range is then limited to 53 dB in this example, which is clearly lower than its IT CCD counterparts. Only if the reset level of the floating diffusion before charge transfer is used as a reference for the photosignal, it is possible to cancel the kTC noise of the sense node through CDS and reach similar dynamic range as IT CCDs.

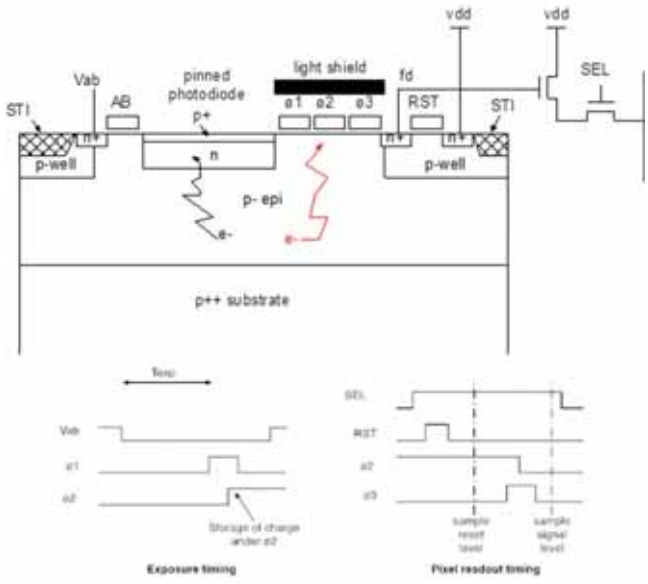

FIGURE 4. CDS charge domain global shutter pixel and timing

Charge domain global shutter pixels

FIGURE 4 shows a charge transfer pixel [1] with correlated double sampling and its timing scheme. In addition to the 5T GS pixel structure, two extra transfer gates ø2 and ø3 have been added. The signal is transferred synchronously in all pixels of the array to gate ø2 after exposure. During readout, this charge packet stored under ø2 is transferred to the floating diffusion row-by-row. The floating diffusion is sampled before and after charge transfer in a CDS scheme, and hence reducing read noise. Read noise of 4.8 e- RMS [2] and 3 e- RMS [3] have been reported with this structure. Shutter efficiency of such pixel is limited, since some photocharges generated in the substrate may be collected directly by the storage gate ø2 rather than by the photodiode. [3] reports a shutter efficiency of 99.96%, which is again limited by charge diffusion and leakage current under transfer gate ø1.

It is clear that CDS and global shutter require two memory elements in the pixel. In this case, the floating diffusion and gate ø2 are these two memory elements. Variants of this structure have been proposed, mainly to reduce the area required for charge transfer and storage: a combined ø1/ø2 gate with two different potentials under it [2], a compact 'pump gate' replacing ø1/ø2 [3] or a structure where ø2 is replaced by a pinned photodiode [4]. Though offering the best noise performance, the shutter efficiency is not satisfactory for all applications. A second problem remains dark current leakage on the storage node ø2. This storage gate is typically a surface channel device (except in [4] where it is a pinned photodiode). For lowest leakage, the storage device should be a buried channel device. But a buried channel device has lower charge storage capacity per unit area, which may limit the minimum possible pixel size.

Voltage domain global shutter pixel

FIGURE 5 shows a GS pixel structure counting 8 transistors and two in-pixel capacitors. This is a voltage domain global shutter pixel that memorizes not only the signal level but also the reset level of the floating diffusion in the pixel on a capacitor behind the first buffer amplifier. The pixel of Fig. 5 shows two storage capacitors that are connected in series but other configurations can be considered where the storage capacitors are connected in parallel or in cascade. This series connected approach resulted in the most compact pixel design. Timing is also shown in Fig. 5. The image acquisition cycle starts with an exposure of the pinned photodiode. At the end of the exposure period, the reset level Vreset is first sampled on C2, after which charge is transferred to the floating diffusion FD. Then the signal level Vsignal is sampled on C1. During readout, first the reset level is read out from C2. Then C1 and C2 are shorted. Since C1 and C2 are equal in capacitance, the signal read

after shorting both capacitors is (Vsignal + Vreset)/2. The readout circuit, present typically in the column amplifier of the image sensor, calculates the difference between both pixel readings, and amplifies the signal again so that Vsignal – Vreset results.

Fig. 5 shows two timing modes. In mode 1, the S2 pulse remains on during sampling of the second sample Vsignal of the pixel. In mode 2, S2 is opened again before sampling. Mode 1 contains an asymmetric gate-source cross-talk between the two samples. This causes an extra offset between both readings and increases fixed pattern noise by approx. 30%. However, temporal read noise is lower. It can be shown that the temporal read noise of the pixel is optimum when C1 is equal to C2. In mode 1, the temporal read noise is given by kT/2C where C is the capacitance value of C1 and C2. In mode 2, the read noise is kT/C. A more complex model including noise of in-pixel transistors has been made. Read noise depends strongly on the size of in-pixel capacitors. For larger pixels, a larger capacitance can be made, and lower read noise can be reached. A 5.5 µm pixel with two in-pixel capacitors of 16 fF each has been made, resulting in 13 and 10 e- RMS in modes 2 and 1 respectively. A larger 6.4 µm pixel with two in-pixel 36 fF capacitors reached 8 e- RMS. On a smaller 3.5 µm pixel, only 8 fF was available, resulting in a read noise of 17 e- RMS.

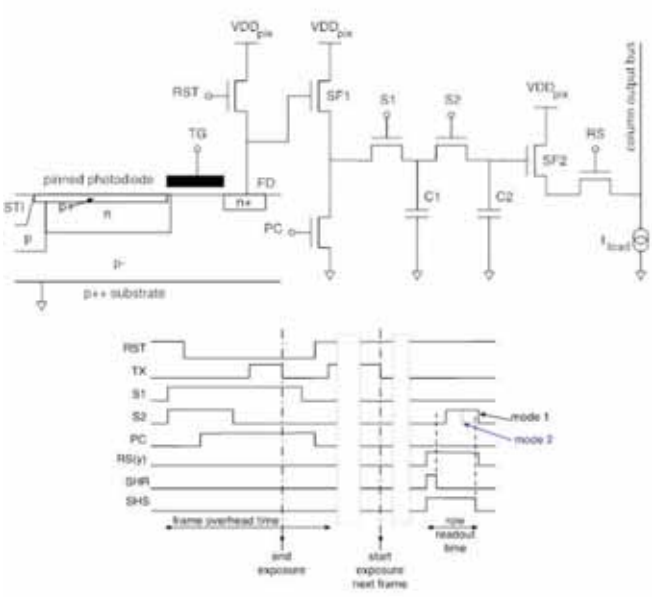

FIGURE 5. Voltage domain global shutter pixel with CDS

Full well charge of the 5.5 µm pixels is limited by the swing on the floating diffusion sense node, to about 13,500 e-. This results in a dynamic range of 60 dB for the 5.5 µm pixels. The 6.4 µm pixel reaches a full well charge of 15,000 e-, which results, together with its lower noise, in 65 dB dynamic range.

Shutter efficiency of this 8T GS pixel structure is excellent thanks to a variety of reasons:

1) the capacitors C1 and C2 are implemented through gate or metal-isolator-metal capacitors, which are unable to collect charges generated in the substrate. Some small contribution of charges collected from the substrate is still possible, through the source/drain junctions of the in-pixel switches S1 and S2. But these junctions do cover only a very small area of the pixel
2) If such charges are collected from the substrate, there is a similar chance that they are collected on C1 or on C2. This creates a common-mode offset error on both the signal and reference samples stored on both capacitors, which is cancelled after CDS.
3) An electron collected on C1 or C2 has less impact on the voltage signal than an electron present on the floating diffusion, by the ratio of the capacitance of the floating diffusion and the storage capacitor. For example, in the 5.5 µm pixels, the floating diffusion is 1.6 fF, and the storage capacitors are 16 fF each. This means that an electron converted on FD causes a signal change of 100 µV, while an electron collected on C1 or C2 causes only a shift of 10 µV.

The reported shutter efficiency for a front-side illuminated (FSI) 8T GS pixel is better than 99.999%. Because the pixel does not rely on light shields and the storage nodes are almost not capable of collecting any charges from the substrate, such pixel can also be used in combination with backside thinning.

Backside illumination and global shutter pixels

Today, backside illuminated CMOS image sensors have been widely adapted in consumer applications. This technology was introduced to improve light sensitivity while pixel pitch could be further reduced, to 1.4 µm and below. The same technology can also help to improve quantum efficiency and light sensitivity of global shutter pixels. Backside illumination (BSI) can also increase the light sensitive spectrum into the near and extreme UV spectrum. These wavelengths are blocked on traditional

front-side illuminated image sensors due to absorption in the inter-metal dielectric layers on top of the silicon. But these wavelengths get important in more and more machine vision applications, for example semiconductor inspection.

Since with BSI, the photocharges are generated from the backside surface onwards, charge diffuse towards the photodiode gets more important. This is why obtaining good shutter efficiency is more difficult than with front-side illumination. Light shields are not very effective, since they don't influence charge diffusion. Also, shutter efficiency now becomes worse for shorter wavelength, since these photons are absorbed closer to the surface and generate photocharges further away from the photodiode. In particular for the charge domain global shutter pixels discussed before, it becomes difficult to avoid diffusion to the charge storage element. A voltage domain global shutter pixel with CDS can keep its good shutter efficiency thanks to the reasons mentioned before, such as the lower impact on the signal when an electron hitting the storage element, and the differential operation of the CDS voltage domain global shutter pixel.

An 8T voltage domain global shutter BSI prototype image sensor has been made and reported [6] with a shutter efficiency of 99.996%, well above the acceptance limit for almost all use cases. Read noise and full well charge, were not changed with backside illumination. QE can be optimized to the desired wavelength range by an optimized anti-reflective coating.

Scaling of global shutter pixels

The 8T pixel structure contains a lot of components (8 transistors, 2 capacitors) and a significant amount of interconnect routing. The smallest possible pixel pitch in 0.18 µm CMOS is around 5.5 µm. To develop smaller 3.5 µm pixels the following approaches were taken:

1) The IC technology is switched for a smaller geometric node. CMOSIS developed pixels in a process with 110 nm front-end and 90 nm back-end design rules. This process was initially developed for 1.75 µm shared 4T pixels and allows narrow interconnect pitch. Also the height of the interconnect stack is reduced, which improves the optical performance of the pixel such as quantum efficiency and angular pixel response.
2) Pixel sharing is employed to share the first source follower in the pixel. Interconnect routing is shared to select pixels from 2 adjacent rows to 2 vertical column busses.

More details are described in [7]. In spite of the scaling, a dynamic range of 58.5 dB is reached on a 3.5 µm global shutter pixel, with a noise level of 17 e- RMS and a full well charge of 14,800 e-. Quantum efficiency is 46% at 550 nm.

Conclusions

CMOS sensors with global shutter pixels can only compete with IT-CCD devices in case when the pixel allows correlated double sampling (CDS), in order to keep the temporal read noise low. Mechanisms similar to smear in a CCD cause a degradation of shutter efficiency on the global shutter pixels, which must be dealt with effectively in pixel design. One solution is a voltage domain global shutter pixel. Several pixel implementations have been discussed, and pixel specifications of voltage domain pixels are listed in **TABLE 1**. Charge domain pixels offer lower read noise

TABLE 1. Key specifications of voltage domain CDS global shutter pixels developed at CMOSIS

Device	CMV300	CMV2000 CMV4000 CMV8000 CMV12000	CMV20000	Custom	Unit
Pixel pitch	7.4	5.5	6.4	3.5	µm
Full well charge	20,000	13,500	14,500	14,800	e-
Read noise	12	13 (10)	8	17	e- RMS
Dynamic range	64	60	65	58.5	dB
Shutter efficiency	99.998	99.998	99.998	99.98	%
FPN	< 20	< 13	< 30	< 35	e- RMS
PRNU	1	1	1.3	1.2	% RMS
QE (550 nm)	55	60	45	46	%
Dark current (20°C)	100	125	125	85	e-/s

at the cost of decreased shutter efficiency and are more difficult to use with backside illumination. Future developments in global shutter pixels use CMOS scaling for smaller pixel structures, while aiming to at least maintain performance at the values reached today. Backside illumination can be considered, and has been demonstrated already with voltage domain global shutter pixels.

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A fundamental truth of process control

DAVID W. PRICE *and* **DOUGLAS G. SUTHERLAND**

You can't fix what you can't find. You can't control what you can't measure.

This is the first in a series of 10 installments which will discuss fundamental truths about process control—inspection and metrology—for the semiconductor industry. By fundamental, we imply the following:

- Unassailable: They are self-evident, can be proven from first principles, or are supported by the dominant behavior at fabs worldwide
- Unchanging: These concepts are equally true today for 28nm as they were 15 years ago for 0.25µm, and are expected to hold true in the future
- Universal: They are not unique to a specific segment of process control; rather they apply to process control as a group, as well as to each individual component of process control within the fab

Each article in this series will introduce one of the 10 fundamental truths and discuss interesting applications of these truths to semiconductor IC fabs. Given the increasing complexity of advanced devices and process integration, process control is growing in importance. By understanding the fundamental nature of process control, fabs can better implement strategies to identify critical defects, find excursions, and reduce sources of variation.

The first fundamental truth of process control for the semiconductor IC industry is:

> *You can't fix what you can't find. You can't control what you can't measure.*

While it's true that inspection and metrology systems are not used to make IC devices—they do not add or remove materials or create patterns—they are critical for making high-yielding, reliable devices. By finding defects and measuring critical parameters, inspection and metrology systems monitor the hundreds of steps required to manufacture a device, ensuring the processes meet strict manufacturing specifications and helping fab engineers identify and troubleshoot process issues when there is an excursion. Without inspection and metrology, it would be near impossible for fabs to pinpoint process issues that affect yield. However, it's not enough to simply "find" and "measure"—a fab's process control strategy needs to be capable and cost-effective.

Capable inspection and metrology strategies find and measure the defects and parameters that affect device yield. Cost-effective inspection and metrology is performed at the lowest total cost to the factory, where total cost is the sum of the cost of lost yield plus the cost of process control.

First, make it capable

If you can't find it, you can't fix it. At the heart of this truth is the understanding that, above all else, a fab's inspection and metrology strategy must be capable. It must highlight the problems that are limiting baseline yield. It must also provide actionable information that can enable fabs to quickly find and fix excursions (**FIGURE 1**).

We emphasize this need for capability first because we have observed that some fabs are too quick to

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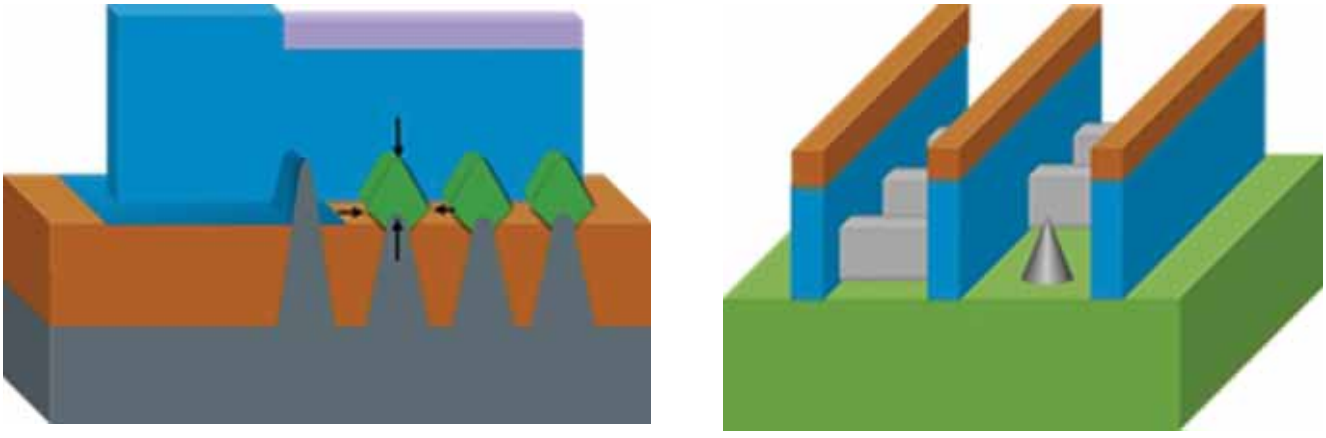

FIGURE 1. You can't fix what you can't find. And you can't control what you can't measure. Left: P-MOS SiGe critical dimension measurement. Right: Fin patterning particle leading to a Fin Spire defect at post dummy gate etch. Source: KLA-Tencor

sacrifice capability for cost reductions. No strategy is cost-effective if it doesn't accomplish its fundamental objective.

Below are specific questions that can help fab management evaluate the capability of its process control strategy:

- Are you finding all sources of your defect-limited yield? Are you finding these in-line or at end-of-line?
- Does your defect Pareto have sufficient resolution of the top yield-limiters in each module to direct the most appropriate use of factory engineering resources?
- Have you fully characterized all of the important measurements and defect types (size range, kill ratio, root cause, solution)?
- Do you understand the most probable excursion scenarios? What is the smallest excursion that you absolutely must detect at this step? How many lots are you willing to have exposed to this excursion before it is detected?
- Are you inspecting and measuring at all the right steps? Can you quickly isolate the point of formation for excursions? Can you quickly disposition potentially affected lots?
- Does a particular defect signature become confused by defects added at subsequent process steps? Or do you need separate inspections at each step in order to partition the problem?
- Do you have overlapping inspections to guard against the high-frequency, high-impact excursions?
- What is the alpha risk and beta risk for each inspection or measurement? How are these related to the capture rate, accuracy, precision, matching and more?

Then, make it cost-effective

Once a capable strategy is in place, then a fab can start the process of making it cost-effective. The best known method for optimizing total cost is usually adjusting the overall lot sampling rate. This is generally preferred because the capability remains constant. In some cases, it may be possible to migrate to a less sensitive inspection (lower cost of ownership tool or larger pixel size); however, this is a dangerous path because it re-introduces uncertainty (alpha/beta risk) that reduces a fab's process control capability. This concept will be discussed in more detail in our next article on sampling strategies.

Finally, it is worth pointing out that it is not enough to implement a capable strategy. The fab must ensure that what was once a capable strategy, stays a capable strategy. A fab cannot measure with a broken inspection tool or trust a poorly maintained inspection tool. Therefore, most fabs have programs in place to maintain and monitor the ongoing performance of their inspection and metrology tools.

By optimizing process control strategy to be capable and cost-effective, fabs ultimately find what needs to be fixed and measure what should be controlled—driving higher yield and better profitability.

The semiconductor industry: Out in front, but lagging behind

TOM MARIANO, *Foliage, Burlington, MA*

Capital equipment suppliers must provide advanced analytical systems that leverage data generated by their tools to help their fab customers address the challenges of Big Data and advanced analytics.

We live in a highly-connected world. Powerful intelligent devices for personal and home use are pervasive and proliferating at an accelerated rate and will number in the tens of billions in the years to come. These devices are connected to powerful back-end software creating intelligent systems. The semiconductor industry is a major enabler of these intelligent systems. The industry's drive to adhere to Moore's Law has resulted in extremely low-cost memory, tremendous computing power and high-speed connectivity, in packages that are low cost and have low power consumption.

These device-level advances when combined with innovations in information technology such as Cloud computing, Big Data and advanced analytics are at the core of intelligent systems that impact our daily lives. Glancing at my phone right now, I see iTunes, YouTube, LinkedIn and my home and work email—all evidence of Cloud computing. Big Data and advanced analytics are widely used for such things as targeted advertising, insurance and credit underwriting, fraud detection, healthcare research, legal discovery, social network analysis and many other areas that impact our lives. Cities around the world, from Da Nang to Fort Lauderdale are applying technologies such as advanced data and analytical tools, cloud-based services and integrated wireless services to make life easier for everyone.

In the manufacturing industry, there is a parallel revolution also leveraging the same advanced information technologies – intelligent manufacturing. The adoption of robotics and automation in manufacturing is increasing precipitously. The use of 3D printing is exploding. Manufacturing machines are becoming more and more intelligent and warehouse automation is rapidly expanding. Intelligent manufacturing systems are dependent on data—data that is shared and acted upon at all levels.

This is leading to changes on the data side as supply chains are being automatically linked for improved tracking and coordination. Advanced analytics are enabling real-time decision making on the factory floor while tool diagnostics are often happening remotely and sometimes automatically. The semiconductor industry has led other manufacturing sectors in the adoption of highly automated, intelligent manufacturing, but is lagging in the application of new information technologies.

Out in front

The need for smaller feature sizes and more aggressive cleanliness and particle-count metrics is the very nature of the semiconductor industry. The accuracy and precision requirements of this complex microfabrication process has always necessitated its isolation from direct human intervention. This necessity to isolate semiconductor wafer processing from humans and the drive to adhere to Moore's Law has pushed

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advanced technology into the semiconductor manufacturing process resulting in significant progress in automation and optimization of process and production. Clean processing has driven the proliferation of wafer-handling automation within process tools. Wafer-handling robot arms in vacuum and atmospheric tools are standard today. Meanwhile, Moore's Law played the primary role in wafer size increases and the automation that is present outside of the process tools.

Starting in the 200mm generation, mini-environments (i.e., SMIF pods) as a means to isolate wafers from particles during inter-tool transport became standard. The standard carrier with twenty-five wafers, and its resulting high weight along with the increased fab throughput demands driven by Moore's Law, led to the propagation of inter-bay automated material handling systems (AMHS). The movement of wafers from one processing bay to the next became automated. This trend continued in the 300mm generation with larger and heavier standard carriers (i.e., FOUPs). And with this generation came standardized intra-bay AMHS. Process tool to process tool delivery of wafers was automated as a result. Fully-automated, chamber-to-chamber automation in the semiconductor industry (at least for front-end processing) is decades ahead of other discrete manufacturing industries. In recent years, there's been an acceleration of robotics within non-semiconductor sectors, but most of these industries are only scratching the surface compared to the semiconductor industry concerning material handling automation.

The semiconductor manufacturing process has also made major advances in data automation. The manufacture of computer chips is extremely complex requiring hundreds of process steps, each affecting change to the silicon wafers at a microscopic level. Also complicating the process is the need for producing multiple products in the same fab with overlapping, but also divergent process steps. This complexity drove the need and proliferation of manufacturing execution systems (MES) in semiconductor processing. Process

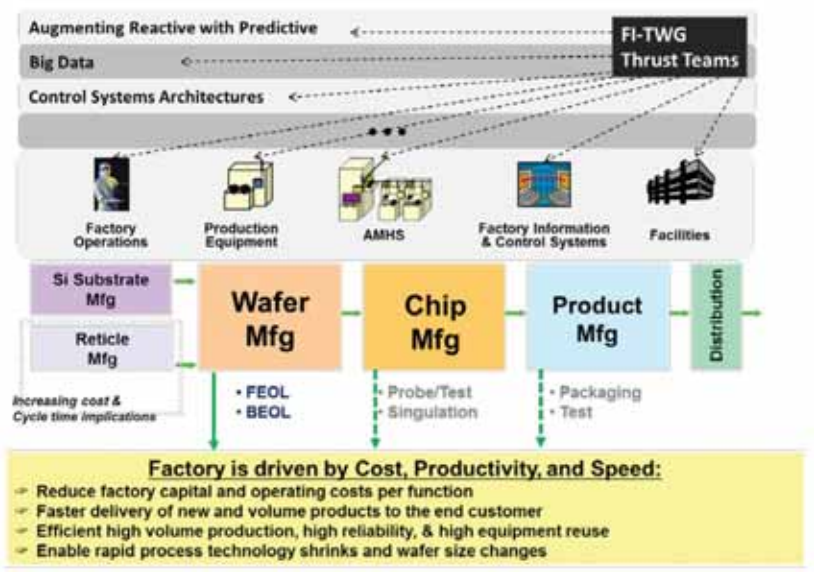

FIGURE 1. Factory integration scope (Source: ITRS).

tool data connections, so-called tool automation is also commonplace, enabling automatic recipe download and tool configuration, remote control and automated data collection. Advanced Process Control (APC) is widely used to improve yield.

And finally, due to the re-entrant repetitive WIP flow required by wafer processing, sophisticated WIP scheduling and dispatching systems exist to optimize, as much as possible, fab throughput and cycle time in pursuit of Moore's Law. When it comes to data, semiconductor manufacturing is out in front of other discrete manufacturing industries - by far it seems. In the semi industry, the combination of one hundred percent of processing tools connected and automated with metrology feedback loops via APC is not something you see in other discrete manufacturing sectors.

But lagging behind

Recent actions by several large well-known companies emphasize the escalating trend toward intelligent manufacturing. Apple, moving toward fully automated production lines in the U.S., allocated $11B to robotics and automation technology. General Electric announced a $3B investment in the "Industrial Internet of Things." Google acquired eight robotics companies in 2013. And, Amazon bought Kiva Systems, a warehouse automation company for $750M. Similar actions

echoed by thousands of less well-known companies, albeit predominantly on a smaller scale, are also playing a role in the acceleration of intelligent manufacturing. The semiconductor industry is out in front relative to material handling and data automation. However, massive non-semi investment in intelligent manufacturing information technologies is leaving the semi industry lagging far behind.

The use of Big Data, coupled with advanced analytics in the manufacturing process is another area where the semiconductor industry has a long way to go. The amount of data that is needed to be tracked in semiconductor processing is exploding. As design rules shrink to below 32nm critical dimension today and 14nm in the near future, both feature density and the number of transistors per chip experience significant growth. More features per chip translate to:

- taking more measurements
- higher lithography refraction rates resulting in higher error rates
- exceptions requiring more data to resolve and lower yields meaning more exceptions per wafer (and wafer layer)

As a result, the retention period for these measurements (e.g., to measure tool drift over time) is increased, and the volume of data to be handled by analytics (across lots and tools over time) is magnified considerably. The delayed, but looming transition to 450mm will create a geometric multiplication of the data handling needs.

The value in this massive amount of rapidly created data is in the insight and decision making that can be derived from the data. Here is where the issues lie. Semiconductor manufacturing takes advantage of APC, and in many ways, this is more advanced than a lot of other industries. However, the International Technology Roadmap for Semiconductors (ITRS 2013) emphatically states:

"...a truly comprehensive APC manufacturing strategy is not yet reality, nor is a portfolio of sensors and metrology tools to support complete factory-wide deployment, particularly given the profound changes in materials, processes, and device structures expected for future technology generations. The benefits already realized from APC are driving the development of new sensor technologies and associated control software, which will allow factory-wide comprehensive solutions to be realized in the near future."

Integrated metrology implementation also presents difficult challenges - metrology tools included as subsystems of process tools. Usually, fabs are designed as a network of tools that each performs one specific function, not multiple functions. This assumption constrains material handling, data flow, MES, etc. Sophisticated, real-time data management and analytics are needed to take advantage of in-situ measurement data with minimal (or zero) impact to tool throughput **FIGURE 1** illustrates factory scope and **FIGURE 2** shows factory targets as defined by the ITRS.

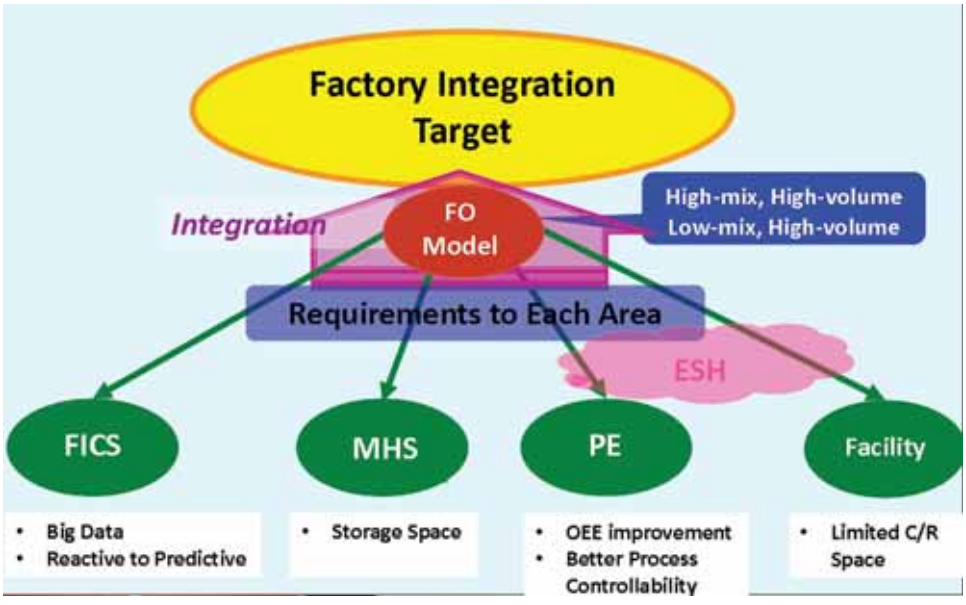

FIGURE 2. Factory integration target (Source: ITRS).

Also, in the new "Big Data" section of the ITRS, expected data volumes are shown as "TBD" which is very telling. The units are in Terabytes per day and the possibility that fabs will have to deal with multiples of Petabytes of data is very real. Beyond APC there are other significant data challenges such as traceability to

lot and die, test data tracking, predictive tool maintenance and Fault Detection and Classification (FDC). The industry is just starting to grapple with how to effectively leverage Big Data and advanced analytics in the semiconductor manufacturing process.

There is a very complex variable interaction problem in semiconductor manufacturing. Going forward, a greater variety of data will be collected at a rapid pace. In many cases, interaction models do not exist today. This will require experimentation and experience to understand interactions in order to derive insight and value from the data. Advanced analytical techniques exist, but determining the right techniques to use for certain decision making will be extremely difficult. Infrastructure and cost are two other issues. The collection, storage and processing of large amounts of data require expensive infrastructure. Support of high data throughput process tool connectivity could require new MES and cell controller architectures. Security is also an issue. Sharing data with capital equipment suppliers and other suppliers will be necessary to derive decision-making value from the data. However this data is highly sensitive and closely guarded by the fab. Similarly, the medical industry is challenged with how to share data aggregated from patient medical records with device makers whose focus is improving patient outcomes in a way that protects patient confidentiality.

Not all the challenges fall solely on the fabs. Capital equipment suppliers have an opportunity to leverage their process and measurement tools to develop solutions to help solve the Big Data, analytics challenges of their customers – the fab operators. Understanding by these suppliers of the environment in which their tools reside will be critical. The system software that runs these tools also becomes more important. The continued development of new process controllers and add-on sensors may require an updated system design paradigm. The data acquisition and management systems of these platforms also need a fresh vision - one that can be implemented in their process and material handling control architectures. Capital equipment suppliers will need to rethink their system design and potentially their business models to leverage the value of the data that their tools can provide.

Conclusion

Semiconductor manufacturing, driven by the need for clean processing and Moore's Law, leads most other manufacturing sectors in implementing automation and advanced process control. However, large, well-known manufacturing companies outside of semi are making huge investments to progress the use of advanced information technologies in manufacturing because they realize the advantages to be gained. Leveraging technologies capable of handling large amounts of data will provide deeper insights into their manufacturing processes.

The semiconductor industry is poised to take advantage of advanced information technologies. Yes, there is a long way to go and challenges abound. However, the potential value to each fab in addressing key operational metrics such as increased yield, reduced cycle time and increased throughput is significant. The sheer complexity of the interactions of variables in the semiconductor process and the massive amount of data to be collected, stored and analyzed are significant challenges. And, the eventual move to 450mm will compound the huge data volume and velocity issues. I believe that the solution is a collaborative approach – not only fab operators working with software solution providers deploying fab systems, but also in close collaboration with capital equipment suppliers.

Capital equipment suppliers must provide advanced analytical systems that leverage data generated by their tools to help their fab customers address the challenges of Big Data and advanced analytics. It is these companies, who understand best the process data that the equipment can track, interpret and communicate. The semiconductor industry has a long history of fab companies working with their suppliers to further the goals of the industry as a whole (e.g., SEMI standards and other consortia). This effective collaboration model can be used to leverage advanced information technologies for improving the manufacturing process. Semi is lagging, but innovation, drive to success attitude, and organization of the industry will make up the ground quickly.

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SEMI advocates for the industry in Washington

Jamie Girard, senior director, Public Policy, SEMI North America

With changes coming in Washington, SEMI has important work ahead supporting the innovators and job creators of this country. Advancing the goals of its members, SEMI advocates legislation in congress, targeting passage of the Commerce, Justice and Science Appropriations Act, increases to NSF and NIST funding and changes to R&D tax credits.

As mid-term election season heats up throughout the country, lawmakers' minds have begun the biennial shift back toward the electorate and the promise of a frenetic sprint to November. However, there remains important work to be done in Washington which stands to have a significant impact on the SEM industries. On December 10, 2013, Congress passed the Bipartisan Budget Act, a two-year deal which laid out the broad parameters for appropriators to build from in formulating fiscal year 2015 spending bills. Congress is now rushing to pass the 12 separate appropriations bills under regular order.

Last week, the House passed the FY 2015 Commerce, Justice, and Science Appropriations Act—the funding legislation with direct implications for many SEMI members. The bill includes $7.4 billion in funding for the National Science Foundation (NSF), representing a 3.3 percent increase over the FY 2014 level. This funding supports programs that foster innovation and U.S. economic competitiveness, including funding for research on advanced manufacturing, cybersecurity, and STEM education. Additionally, the bill includes $856 million for the National Institute of Standards and Technology (NIST), approximately a one percent increase from the previous year. NIST's laboratories, research and standards development, and manufacturing services have proven crucial to boosting American innovation and competitiveness. The Senate is expected to consider the CJS bill in June and we are hopeful that these levels will be realized in the final version of the bill.

SEMI testifies at house manufacturing caucus.

Another important item moving through the legislature is the R&D tax credit. On April 29th, the House passed a permanent R&D tax extension without offsets. The R&D credit expired at the end of last year along with more than 50 other tax breaks but the $156 billion House bill extended just the R&D tax provision. This is a novel approach as the R&D credit has been extended on a short-term basis for nearly 30 years. The Senate is taking a different approach to tax policy, considering shorter extensions through a legislative vehicle called the Expiring Provisions Improvement Reform and Efficiency (EXPIRE) Act, which passed Committee in early April. SEMI has supported the implementation of a retroactive R&D tax credit in Washington throughout the year and continues to advocate for immediate action on this legislation to reduce business uncertainty for our members.

It is imperative Congress secure passage of an appropriations bill for Science-related items, as well as a renewal of the R&D tax credit, before the election season hits full swing. While both issues could be considered in a lame duck session of Congress, the murky period following mid-term elections has provided few safe bets in years past. These provisions will help direct structural benefits to some of the most innovative companies in the country – and our best job creators. For that, SEMI will continue to work to advance these goals in Washington. If you have questions about SEMI government affairs activities, please contact Taylor Sholler, manager of U.S. Public Policy, at Tsholler@semi.org.

JAMIE GIRARD, *senior director, Public Policy,* **SEMI NORTH AMERICA**

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