# The Role of Direct Step-on-the-Wafer in Microlithography Strategy for the 80's

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Dramatic increases in packing density and cost/performance have been largely achieved by innovative design, an approach now reaching its limit. Direct Step-on-the-Wafer (DSW), the newest microlithographic technique, is the means to achieve future gains in circuit densities and cost/performance. DSW, described in the paper, is the technique whereby reduction of line widths from 5 micrometers to less than 1.0 micrometer is being commercially realized.

TODAY, IN CHARTING PRODUCTION strategy for the near- and long-term future, IC manufacturers focus on economically producing smaller device structures. The dramatic increases in packing density and cost/performance during the last decade were achieved largely through clever design. This approach appears to be nearing its limits. The concern and the burden for future gains in shrinking geometries is being transferred to microlithography. It is in the microlithographic process where reduction of line widths from 5 micrometers to under 1.0 micrometer in approximately a decade is the desired goal. At the same time the cost per logic function must also be reduced.

The production of smaller device structures depends on improvements in many areas, but particularly it depends on development of new processes and higher resolution imaging equipment. This paper will review the capabilities of the major imaging equipment alternatives available today. Special emphasis will be given to the new technique of direct step-on-the-wafer.

The major alternatives being considered today are shown in Table I. The present role for each method is shown in Figure 1. Note that many of these equipment functions complement each other; few are mutually exclusive. The decision on equipment choice is not simply one method or another. The person planning manufacturing strategy must decide which equipment choice will best fit his company's needs. A mix of equipment choices will surely be the result.

For high density VLSI devices, Table II shows the likely microlithography needs over the next decade. The important variable here is feature size. Roughly a 2X shrink every three to five years is required. This rate of change, if realized, could give us a 7 millimeter square, 1024K bit dynamic random access memory by 1985 using 1.4 to 0.7 micrometer geometries.

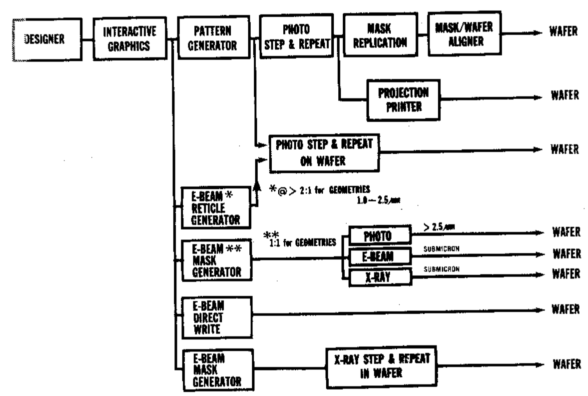


*Fig. 1—Role of various imaging techniques.*

**Table I—Microlithography Wafer Imaging Alternatives**

- Contact printing
- Proximity printing
- 1:1 Projection (whole wafer)
- 1/M Step and Repeat projection
- E-Beam direct write
- X-ray proximity printing (whole wafer)
- X-ray proximity printing (step and repeat)

**Table II—Future Needs for Lithographic Systems**

| Criteria | 1980 Need | 1985 Need |
|---|---|---|
| Minimum geometry | 2$\mu$m | 1$\mu$m—submicron |
| Size control | 5-10% | 5-10% |
| Die size | 3-20mm | 2-20mm |
| Wafer Size | 100-125mm | 100-150mm |
| Accuracy | 0.5$\mu$m | 0.5$\mu$m |
| Precision | 0.25 $\mu$m | 0.125$\mu$m |
| Turn-around/ new design | Days | Days |
| Return on investment | 2 yrs | 2 yrs |

**Alternate Methods**

Electron beam writing techniques and x-ray printing have been carefully examined as ways to generate such lines in wafer production.

Electron beam equipment has demonstrated its usefulness as an R&D tool for development, and where minimum turnaround time for prototype devices is the major consideration. But electron beam direct writing of wafers is still extremely costly, running 10 to 100 times more expensive than current production technology. Even the production of 1024K memories today would not justify such production expenses. Of course, today's wafer process technology prevents such an application anyway. As developments at GCA/Burlington Division and elsewhere improve electron beam's production economics and process possibilities, we believe the electron beam will find a useful role in large scale wafer production of certain devices, but this will not happen for at least five years, and probably not until after 1985. In the meantime, commercially available electron beam systems will remain useful for research and development, mask making, and reticle pattern generation, but not for wafer production.

X-ray printing technology, however, is only a research tool today. Significant problems with masks, wafer stability, and throughput limits remain to be solved. While x-ray printing has great potential, much more needs to be learned about its real usefulness before it can be applied to wafer production on a large scale.

Where does this leave us? Will photo-optical systems do the job? Four years ago many said "no." Today the answer is "yes." The turnaround is due to a recognition of the realities of electron beam economics and the successful development of production oriented direct step-on-the-wafer optical systems.

Figure 2 shows nominal 1 micrometer lines in 1 micrometer of AZ1370 photoresist over a 1 micrometer oxide step. This gives an idea of the resolution capabilities of such systems. Figures 3A-3F show submicron features created by P. Tegreat at E.F.C.I.S. Figure 3G shows similar definition over a 10 millimeter diameter field done on the Thompson LM601 at Siemens. Several visitors to our 4800 DSW Wafer Stepper™ at GCA/Burlington have produced 0.8 micrometer lines in 1 micrometer of resist on 0.5 micrometer of oxide over the whole wafer.

Given that further optical advances are likely, it seems clear that optical projection can meet the small line width needs of VLSI circuits for the foreseeable future. However, such resolution cannot be achieved equally well by all optical imaging techniques.

Table III summarizes the capabilities of the major photolithographic systems. Contact printing has excellent resolution capability. However, in a typical production situation line size control, registration errors, and defect generation are severe problems. These problems make contact printing unsuitable for VLSI production.

Proximity printing sacrifices resolution capability to improve somewhat over contact printing's defect problems. Defects and size control remain as significant problems. VLSI design can no longer afford such problems or the loss of optical resolution associated with proximity printing. This leaves optical production methods as the only method really under active consideration. Currently available projection systems, and a few systems not yet commercially available, are summarized in Table IV.

One-to-one projection systems have been the most popular to date. Their resolution limits have been acceptable, mask costs and defect levels have dropped significantly, and the large field exposure maintains high throughput rates. Present systems, however, are limited in resolution capability to 3 micrometers for usable IC structures. Line width control is also a problem because of the fixed focus and low numerical aperture used in these systems.

A very serious question today is whether one-to-one projection over a wafer's full field in one pass can be improved enough to meet tomorrow's VLSI fabrication needs. Of course only time and experience will give us the final answer, but it is the opinion of the authors that one-to-one wafer imaging cannot be improved sufficiently, and instead high performance motions will be necessary to build up the wafer image out of very high resolution small fields through step-and-repeat exposure. We hold this belief, not for the commercial reasons

*Fig. 2—Positive resist (AZ 1370, 10,000Å) $SiO_2$-1 μm step; (1.0 μm geometry).*

**Table III—Contact and Projection Systems Characteristics**

| Technique | Exposable Area | Min. Use. Feature (μm) | Source Wave Length (λ) | Die Size (mm) | Wafer Size (mm) | Overlay Tolerance | Major Limitations |
|---|---|---|---|---|---|---|---|
| Contact | Wafer | Submicron | Hg Spect. | ----- | 150 | 0.5 - 0.75 | Defect Level, Runout, Mask Cost, Line Variation |
| Proximity | Wafer | 3.0 | Hg Spect. | ----- | 125 | 0.5 - 0.75 | Min. Geometry, Defects, Line Control |
| Projection | | | | | | | |
| 1:1 | Wafer | 3.0 | Hg Spect. | ----- | 125 | 0.5 - 0.75 | Min. Geometry |
| 1:1 | Wafer | 0.4 - 0.5 | 2400 | ----- | 125 | ? | Source, Optics, Resist Availability |
| 10X, 5X, 4X | S&R | 1.8 - 1.25 | 4040 | 10 - 20 | 150 | 0.125 - 0.35 | Accommodation of Wafer Distortion |
| x-ray | Wafer | 0.3 | 4 - 8 | ----- | 100 | 0.5 - 0.75 | Mask Structure, Materials and Registration |
| x-ray | S&R | 0.3 | 4 - 8 | ? | 150 | 0.020 | |

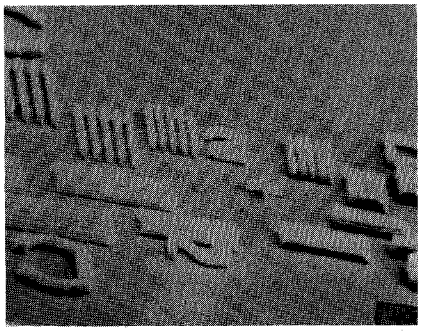

*Fig. 3A—0.35 μm; 0.45 μm; 0.5 μm; 0.6 μm; 0.7 μm nominal line width (half period). (1 μm AZ Resist) 20X, NA = 0.47, 405nm lens.*

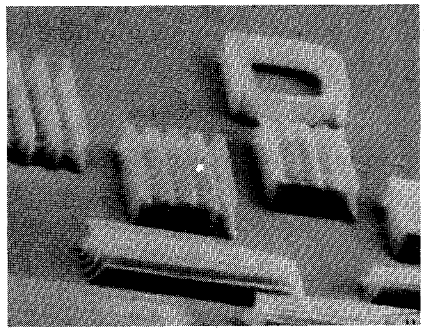

*Fig. 3B—0.3 μm; 0.35 μm; 0.4 μm; 0.45 μm (1 μm AZ resist) 20X, NA 0.47, 405nm lens.*

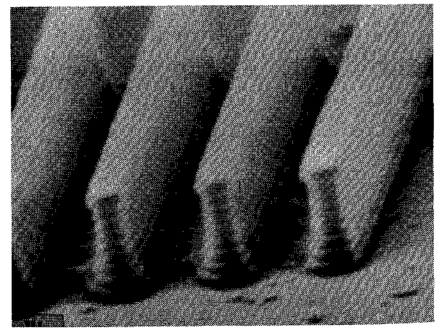

*Fig. 3C—Nominal 0.5 μm lines (1 μm AZ resist) 20X, NA = 0.47, 405nm lens.*

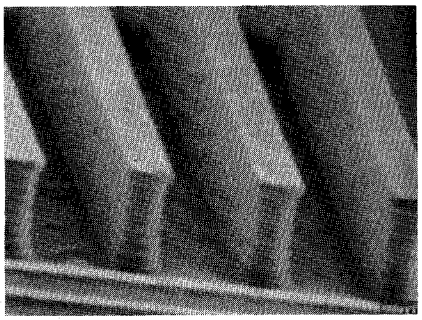

*Fig. 3D—Nominal 0.6 μm line widths (1.0 μm AZ resist) 20X, NA = 0.47 405 nm lens.*

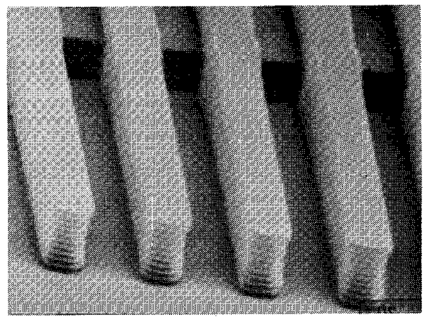

*Fig. 3E—Nominal 0.9 μm lines over 4000Å oxide step (1.1 μm AZ resist) 20X, NA = 0.47, 405nm lens.*

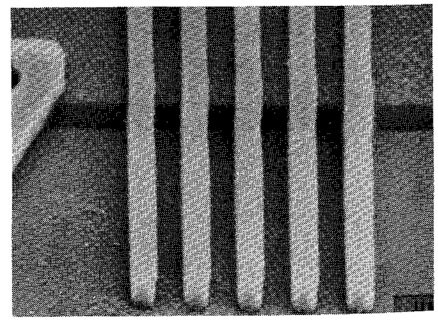

*Fig. 3F—Nominal 1.0 μm lines over 4000Å oxide steps (1.1 μm AZ resist) 20X, NA = 0.47, 405nm lens.*

one might expect, but as a result of examining very carefully the limits of optical projection systems for over fifteen years.

#### Stepping Evolution

The industry-wide method of step-and-repeat generation of photomasks was not always the universal production technique. Early attempts involved single exposure methods, such as fly's eye cameras. Today's acceptance of step-and-repeat has evolved on the basis of correct technical decisions. The same is true for pattern generation of artwork from computer tapes. When single exposure reduction cameras became limited in terms of practical field size and resolution, the idea of mechanically generating device images by combining

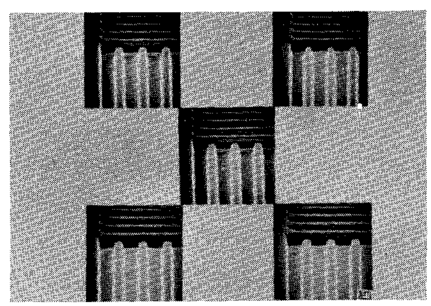

*Fig. 3G—Nominal 1.0 μm lines over 10mm field. 10X, NA = 0.27, 436nm lens (Zeiss) (1.0 μm AZ 1350H resist).*

**Table IV—Projection Printing and Direct Stepping on Wafer**

| Manufacturer | Expos Tech. | Reduct Ratio | Min Geo. | Block Size | Wafer Size | Regis-tration | Thru-put w/hr. |
|---|---|---|---|---|---|---|---|
| P-E | Wafer | 1:1 | 3μm | 94mm | 94mm | 0.25μm | 50-100 |
| Cobilt | Wafer | 1:1 | 3μm | 100mm | 100mm | 0.125μm | 50-100 |
| Ultratech | S&R | 1:1 | 2μm | 10mm | 150mm | 0.25μm | 25 |
| Canon | S&R | 2:1<br>4:1 | 2.0μm<br>0.8μm | 20mm<br>10mm | 75mm<br>50mm | 0.25μm<br>0.125μm | 20 |
| Philips | S&R | 5:1 | 1.25μm | 10mm | 100mm | 0.25μm | ≈ 20 |
| GCA/B | S&R | 5:1<br>10:1 | 2.0μm<br>1.25μm | 20mm<br>10mm | 150mm<br>150mm | 0.25μm<br>0.25μm | 45-80<br>30-50 |
| T/CSF | S&R | 10:1 | 1.25μm | 10mm | 100mm | $3\sigma = 0.3\mu m$ | 5-10 |
| *Censor | S&R | 10:1 | 1.00μm | 10mm | 150mm | 0.2μm | 60 |
| *Optimetrix | S&R | 10:1 | 1.00μm | 10mm | 150mm | 0.1μm | 60 |
| *Electromask | S&R | 10:1 | 1.00μm | 10mm | 150mm | 0.25μm | — |

*At this time, design goals

multiple series of simple rectangular images using a small field, high resolution lens became the accepted method. The same principle is used in today's most advanced electron beam systems to mechanically expand

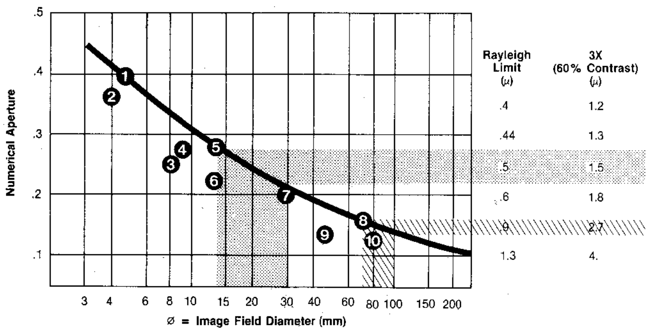


*Fig. 4—Numerical Aperture vs. Image Field Diameter for microelectronic photolithographic lenses.*

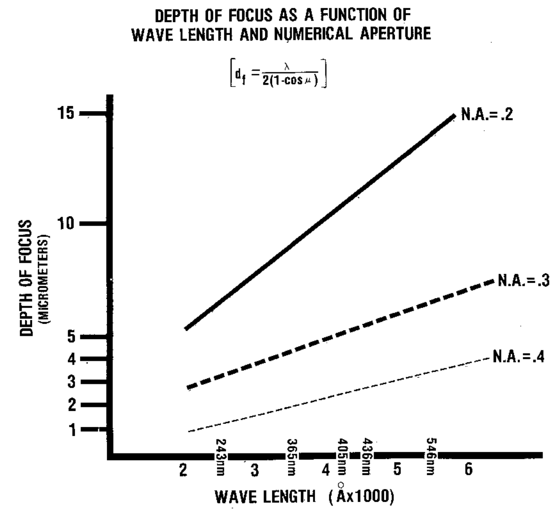


*Fig. 5—Depth of focus as a function of wave length and numerical aperture.*

**Table V—Developments Leading to DSW**

- High resolution lens
- Faster light source
- Faster stages
- Laser controlled X, Y positioning
- Autofocus
- Off-axis alignment

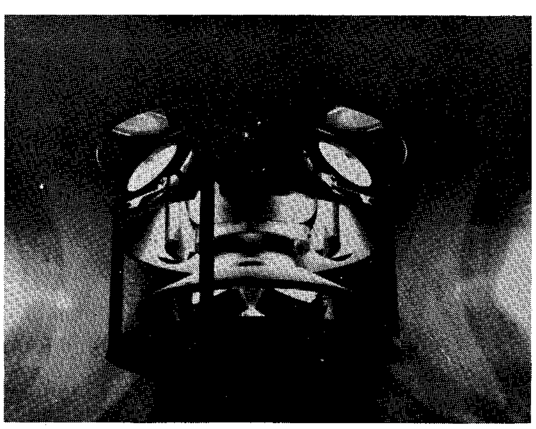

*Fig. 6—Maximus™ illuminator.*

the scanning electron microscope's small field, high resolution capability to a large imaging area. To know when this "mechanics-for-optics" trade-off is appropriate, one must understand the practical limits of projection optics, and the likely capabilities of high performance mechanics.

Figure 4 summarizes a key finding. It shows the relationship between resolution and field size. As field size increases, resolution decreases. Each circled number is a real lens. For example, five and seven are the Zeiss 10X and 5X lenses respectively, and ten is the Perkin Elmer 140 Series Micralign reflective optics. The relationship between field size and resolution is a basic, unavoidable trade-off for refractive or reflecting optics, and represents a statement of practical optical fabrication limits, not theory. The curve moves with time. Gradual improvements in optical fabrication skills have moved performance levels up slightly in ten years (approximately 1.5 times).

Another currently discussed idea is shorter wavelength radiation utilization. In theory, at least, this should provide higher limiting resolution capability for a given optical system. However, Fig. 5 shows one very serious consequence of such a trade-off. As shorter wavelengths are employed, the depth of focus decreases. Even if all other serious technical problems can be solved, some form of local area focusing seems necessary if such a system is to have practical value as a wafer production tool. Again, small area focus (and exposure) will be necessary, and step and repeat coverage of the larger wafer is essential.

Several advances as shown in Table VI were needed before direct step-on-the-wafer could become a practical production tool. Generally, these developments can be summarized as advances in resolution (already discussed), speed and control. Of these three, speed gains have been the most important. Not to be overlooked, however, are other developments including laser controlled x-ray positioning, autofocus, and off-axis alignment.

A new light source, shown in Fig. 6, was essential. The "Maximus 300™" light source used on the Mann 4800 DSW Wafer Stepper™ has improved energy levels at the image plane approximately seven times. This was done by collecting 350-watt lamp radiation in four quadrants, combining the collected radiation in a fiber optic bundle, and optimizing the source size to the 10X reduction lens entrance pupil size. Typical exposure time for 1 micrometer lines in 1 micrometer of AZ1370 photoresist over oxide is now 0.4 sec. This light source is designed to give a partial coherence factor of about 0.7. This has been done to enhance image contrast and resist profiles for the desired 1.0 to 2.0 micrometer line widths. Figure 7 shows the poor definition one gets without partially coherent illumination, and Fig. 8 shows the optical "ringing" one gets if too high a coherence factor is used (here 0.3). The 0.7 factor used in the 4800 DSW Wafer Stepper™ appears to be the appropriate trade-off. The "best" coherence factor, a

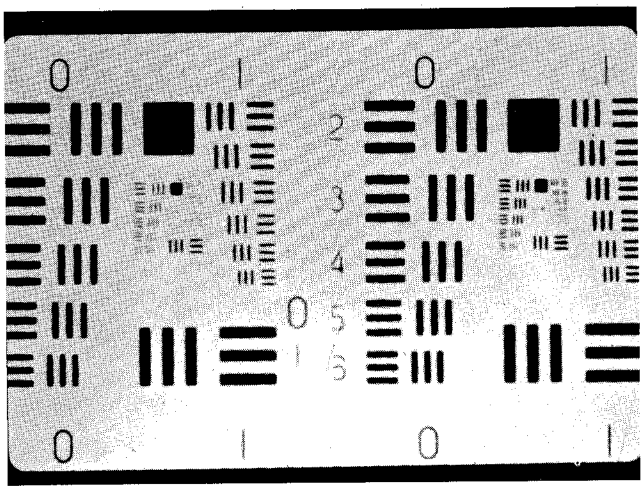

*Fig. 7–Resolution with incoherent illumination (1.0, entraance pupil filled).*

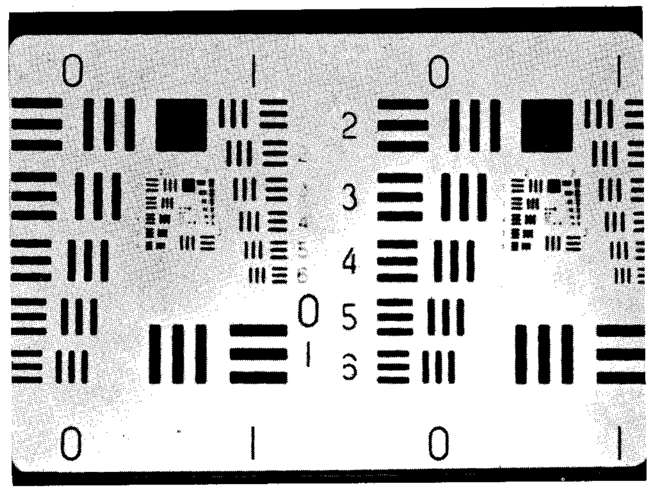

*Fig. 8–Resolution with coherent illumination (0.3 entrance pupil 30% filled).*

function of the lens design, circuit feature size range to be covered, the energy transfer optics and the photosensitive material will vary from one type of system to another.

Fast stages were also essential for achieving production-oriented direct step-on-the-wafer. Increased stepping speed had to be gained while at the same time achieving ± 0.1 micrometer setting precision. Figure 9 shows a typical *x* direction step on the 4800 DSW. Here closed loop laser metering of a coarse and fine stage mechanism (Fig. 10) is used to position the wafer at a new *x, y* location in 0.45 sec. for a 9 millimeter interval. Note the near-critical damping waveform of the servo system. This minimizes settling time.

Laser metering of the wafer stages (Fig. 10) also provides a constant readout of actual wafer location with respect to the projection optics. Least count is λ/16 (0.04 micrometer). The control logic interlocks shutter opening time with the stage settling time so that no exposure is made until the motions are settled at the desired *x, y* location to within a selected tolerance. With this system of stage control we are achieving a 3 sigma positioning error of ± 0.1 micrometer. The laser system also makes possible scaling of stepping intervals which offers several user control benefits discussed briefly later.

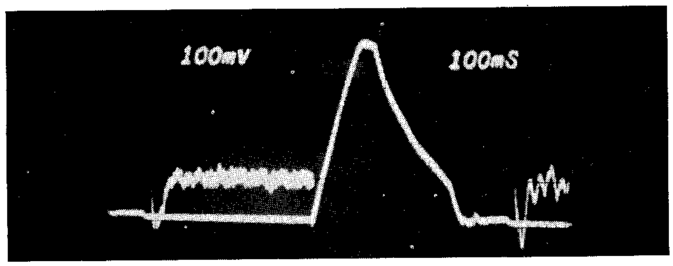


*Fig. 9—Stage stepping interval.*

Step-and-repeat exposure allows one to focus each image center automatically. GCA's Mann 4800 DSW Wafer Stepper™ uses a real time photoelectric sensor (Fig. 11) to monitor the height of the wafer at the center of the exposure and shift the optical column as needed. The lens working distance is 5 millimeters and the column travel range is 635 micrometers. The working least count is roughly 0.1 micrometer, and operating precision is better than ± 0.5 micrometer. This allows for a "crash-proof" design that is user adjustable and one will not drop uncontrolled to impact on the wafer surface. This autofocus feature also affords ready accommodation to typical wafer variations.

The results are significantly improved control of reso-

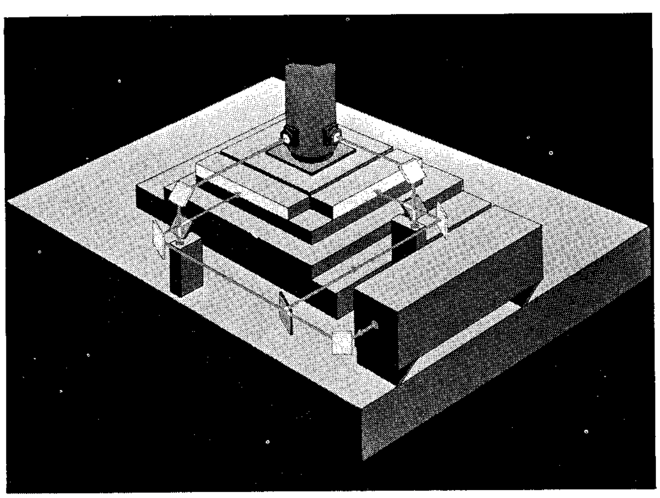

*Fig. 10—Laser interferometric metering.*

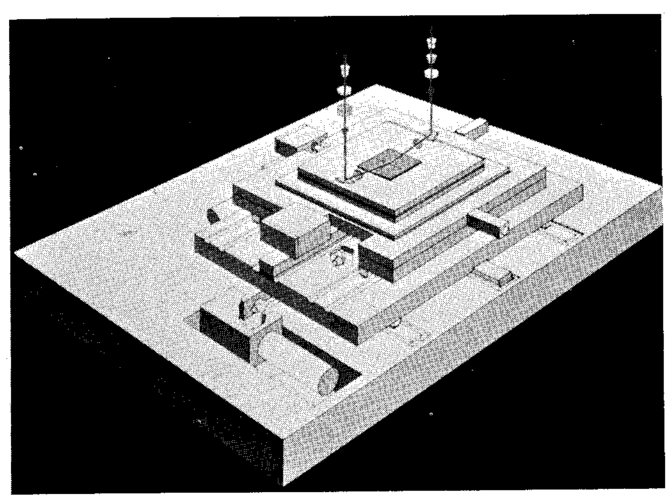

*Fig. 11—Positioning technique and auto-focus.*

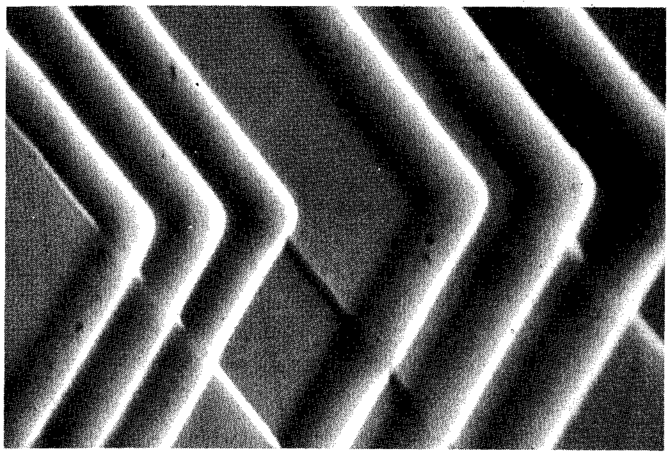

*Fig. 12—HR 200 (8000Å), 2.5 and 3.75 μm geometries.*

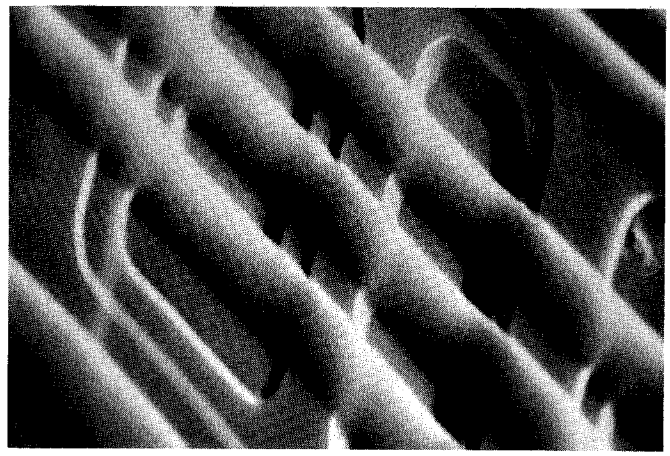

*Fig. 13—Negative resist HR 200 (8000Å), 375 μm geometry.*

lution and line sizes, as can be seen in Figs. 12, 13, 14 and 15.

### Wafer Alignment

Finally, wafer realignment capability had to be developed for layer-to-layer overlay on a wafer. The GCA approach is "off-axis alignment." By looking directly at the wafer (Fig. 16) with an alignment microscope, the projection lens's resolution capability isn't compromised for alignment purposes. Also a 500X, 0.4 numerical aperture, direct viewing capability was possible, since no intervening mask or lens prevents it. The 2.5 inch to 4.0 inch separation of the two viewing objectives makes possible "one stop" alignment of the whole wafer. Direct measurement of each wafer's scale (distortion) error, if any, due to processing, can also be done while at the align position. A high resolution closed circuit TV is provided for remote control of the alignment procedure and to isolate the operator from the temperature and contamination-controlled chamber. Since the alignment marks are in the off-axis microscope, and not on the reticle, the wafer's alignment keys are not destroyed by exposure of the next level.

Table VI shows the estimates of the 4800 DSW Wafer Stepper™ alignment error. Repeated tests show the overall alignment error from layer-to-layer to be ± 0.25 micrometer.

**Table VI—Error Analysis**

| | T.I.R. | Distributed |
|---|---|---|
| 1. Alignment of Reticle | ≤4μ" | ±2μ" |
| 2. Stage Repeatability | ≤4μ" | ±2μ" |
| 3. Alignment of Wafer | ≤12μ" | ±6μ" |
| 4. Thermal effects of + 0.2°F | ≈4μ" | +4μ" |
| | | 14μ" |

$3\sigma$ = 14 microinches 99.7%
$2\sigma$ = 10 microinches 95.0%
$1\sigma$ = 5 microinches 68%
The above are best estimates

Figure 17 shows the present test method. Test procedures have been developed using a universal vernier test target to determine system precision, registration, *x-y* mirror orthogonality, image rotation, optical system reduction ratio, and optical distortion.

The vernier pattern consists of two halves—male and female—which, when interlocked, permit very small "interlocking errors" to be accurately determined without measurement in the classic sense. The vernier halves are shown in Fig. 17. Note that each half consists of two arrays of parallel structures: coarse and fine. The difference in

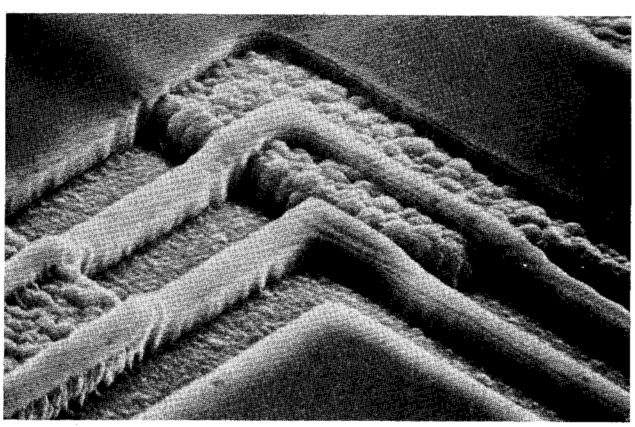

*Fig. 14—Positive (AZ 1350 10,000Å), 2 μm geometry, 1 μm polysilicon topology.*

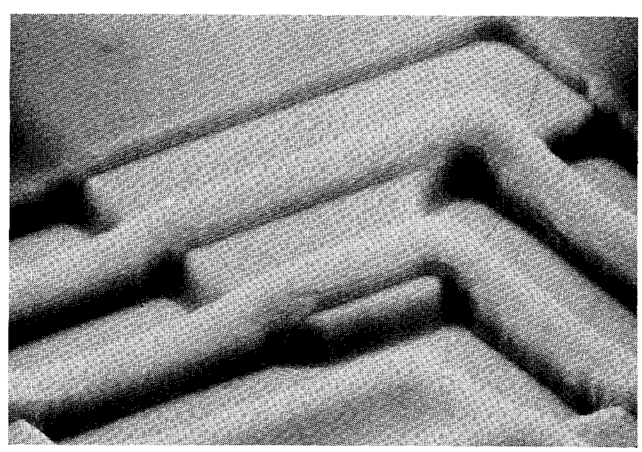

*Fig. 15—2.0 μm geometry, oxide; AZ 1350; (10,000Å).*

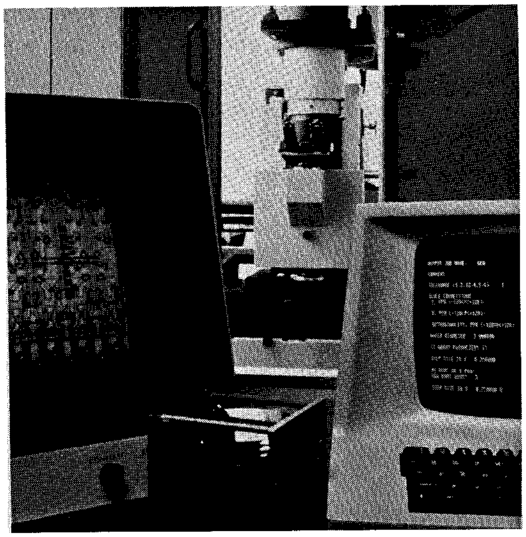

*Fig. 16—Alignment microscope utilizing "off-axis" alignment.*

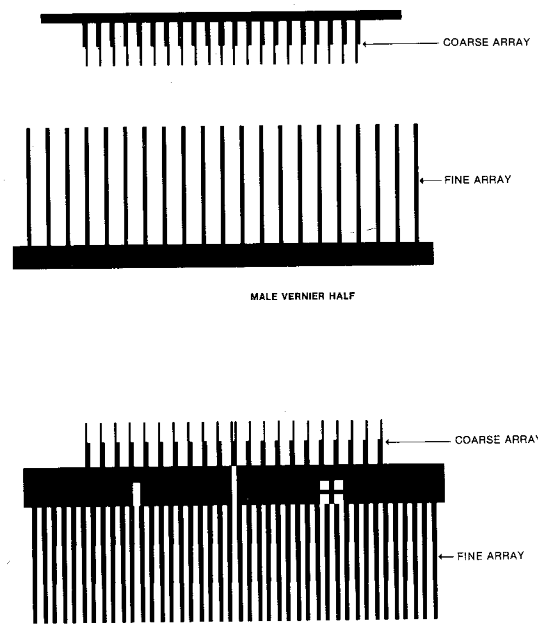


*Fig. 17—Female vernier half and male vernier half.*

periodicity between the male and female coarse arrays is 1.0 μm (at 1X) while the difference in periodicity between the male and female fine arrays is 0.1 μm (at 1X). All arrays consist of ten structures on each side of center. Thus, when the two halves are interlocked, the coarse vernier can measure errors from −10 μm to + 10 μm with a 1.0 μm least count. The fine vernier measures errors from −1.0 μm to 1.0 μm with a 0.1 μm least count. Note that the coarse and fine verniers are not cyclic; that is, they can read an error of say 4 μm, but not 4.1 μm, 4.2 μm, 4.3 μm, etc.

Figure 18 shows the male and female halves interlocked with no error. Note that the "inside" edges of the structures on the female fine vernier are stepped, thus causing a series of three everwidening gaps upon

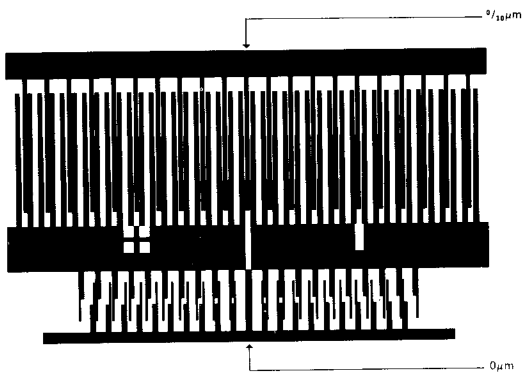


*Fig. 18—Interlocked vernier pattern indicating perfect registration.*

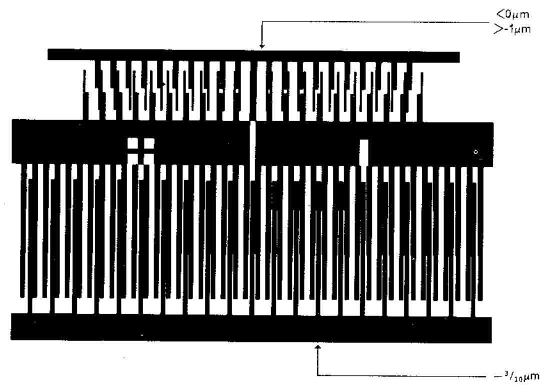


*Fig. 19—Interlocked vernier pattern indicating —0.3 μm error.*

**Table VIII—4800 DSW Throughput and Time Specifications; 4″ wafers.**

| | |
|---|---|
| Wafer Size | 4 inch |
| Step Increment | 360 mils |
| Array, Circular | 89 exposures |
| Resist AZ1370 | 1 micrometer thickness |
| Exposure Time | 500 mililseconds per image |
| Step Time | 430 milliseconds per image |
| **Approximate Times** | |
| Total Exposure | 44.5 sec |
| Total Step | 38.3 sec |
| Load to Expose | 5 sec |
| Expose to Unload | 4 sec |
| Approximate total time | 92 sec |
| Wafers per hour | 39 |

**Table VII—4800 DSW Throughput and Time Specifications; 3″ wafers.**

| | |
|---|---|
| Wafer Size | 3 inch |
| Step Increment | 360 mils |
| Array, Circular | 52 exposures |
| Resist AZ1370 | 1 micrometer thickness |
| Exposure Time | 500 milliseconds per image |
| Step Time | 430 milliseconds per image |
| **Approximate Times** | |
| Total Exposure Time | 26 |
| Total Step Time | 22.4 sec |
| Load to Expose Time | 4 sec |
| Expose to Unload Time | 3 sec |
| Approximate Total Time | 55.4 sec |
| Wafers Per Hour | 65 |

interlocking. This configuration was chosen to aid the user in reading the vernier.

Figure 19 shows the male and female halves interlocked with an error of 0.3 μm.

The end results of these developments provide the stepping and exposing throughput capability shown in Tables VII and VIII. These rates in combination with the improved resolution and control capabilities make direct step-on-the-wafer an economically viable production tool.

Direct step-on-the-wafer does not eliminate all problems. Table IX attempts to summarize its limitations and to indicate needed areas for ongoing direct step-on-the-wafer development. Items marked (with a check mark) are already incorporated into the Mann 4800 DSW system.

Table X summarizes the points made in this paper.

### Conclusion

Overall, the most significant limits for direct step-on-the-wafer methods will be:

1. Cost vs. performance of direct step-on-the-wafer;
2. The control limit placed by topology (step heights) on creation of images over steps.

Cost/performance limits mean direct step-on-the-wafer will find its application in the manufacturing mix (Fig. 1) where its resolution and control benefits pay off. Early indications are that direct step-on-the-wafer is the most economical means available on a production basis for fabrication of scaled-down versions of present circuits such as microprocessors, dynamic RAM's of 64K complexity or greater, advanced bi-polar memories, and bubble memory devices. Topology limits apply to all future wafer fabrication methods, and underscore the need for strong parallel process development efforts if smaller line sizes are to be achieved by any method. When it comes to the necessary equipment strategy, direct step-on-the-wafer will meet future VLSI wafer fabrication needs. Users can be comfortable with 1.25-1.5 μm geometries today and can expect to handle 0.7-0.8 μm geometries tomorrow.

**Table IX—Potential DSW Limitations and Probable Solutions**

- Wafer distortion from process cycles
  - ✓ Scale measuring feature
  - Zone or die by die alignment
- Operator aligning errors
  - ✓ CCTV image
  - ✓ Auto wafer loading
  - ✓ Auto wafer align
- Defects on reticle/wafer
  - ✓ 1/10X imaging
  - Auto reticle changing
  - Smaller die sizes
  - ✓ On-line wafer trac operation
- Process control patterns
  - Include in die image (scribe area)
  - Programmable "aperture" blades at 10X
- Machine to machine matching
  - ✓ Scaling parameters in software (X, Y, 90°)
  - Better testing methods
  - Point by point correction via software
- Wafer non-uniform thickness variations
  - Better material
  - Leveling
- Process development
  - Positive resist use
  - Wafer processing for small features

**Table X—Conclusions and Outlook**

- X-ray Methods
  - —Too early, needs development
- E-Beam Methods
  - —R & D, masks, reticles now
  - —Direct write when ecoonmical (1985 or later)
  - —Not economical today for production
  - —Not needed for today's geometry
- 1:1 Projection
  - —Useful today
  - —Near technology limits (resolution, focus, field size, registration)
- 1/10X DSW
  - —Proven new technology
  - —Capable of doing tomorrow's VLSI devices
  - —Fills niche between today and E-Beam
  - —Significant future technology improvement possible

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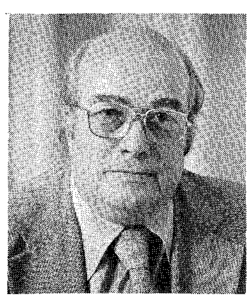

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